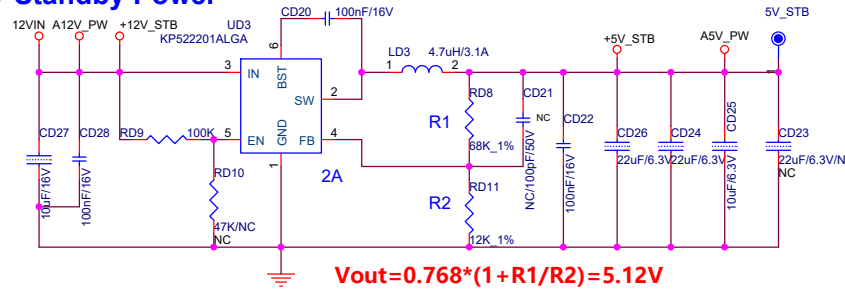
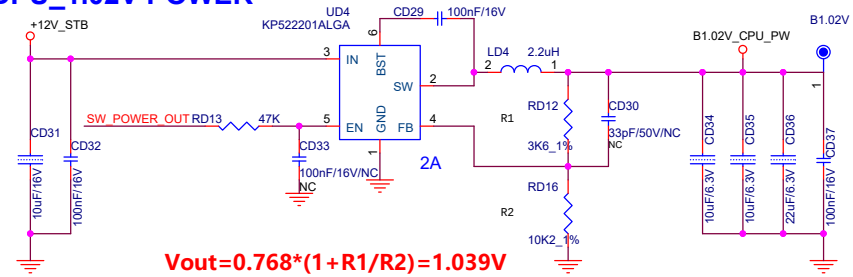


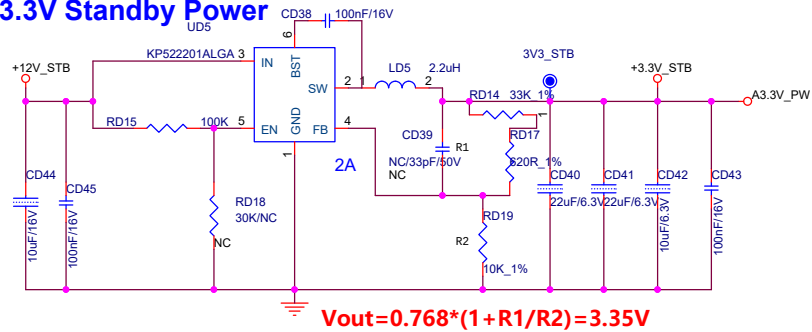
5V Standby Power



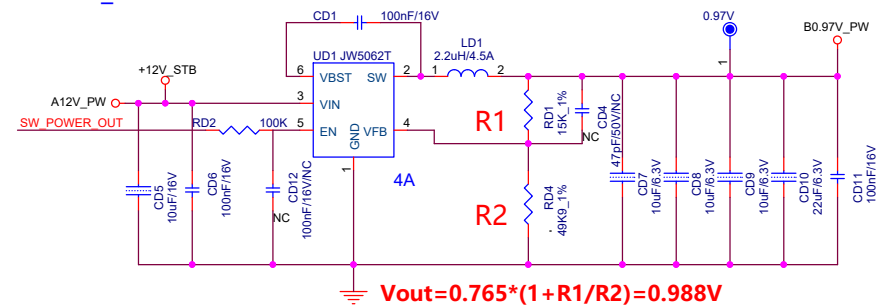
CPU_1.02V POWER



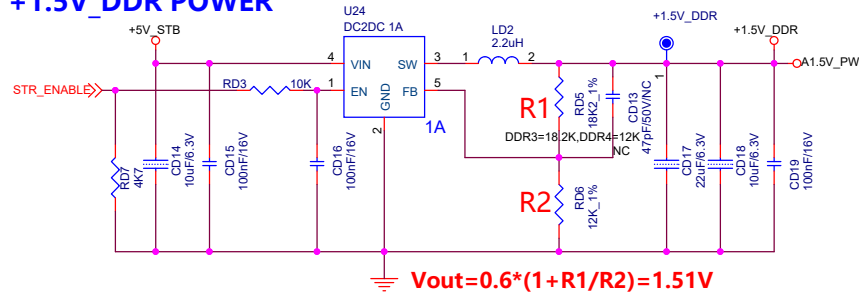
3.3V Standby Power



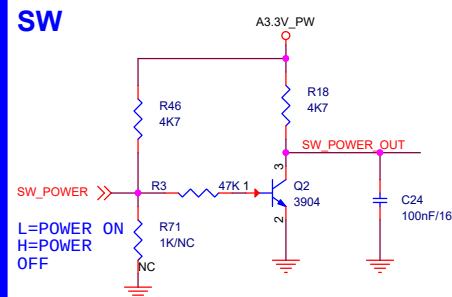
+0.97V_VDDC



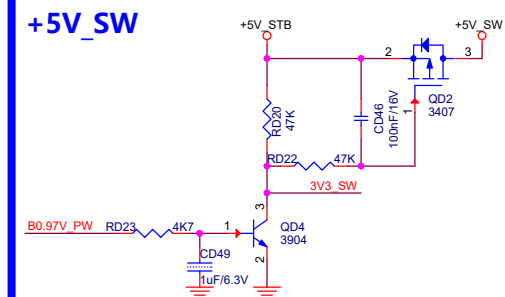
+1.5V_DDR POWER



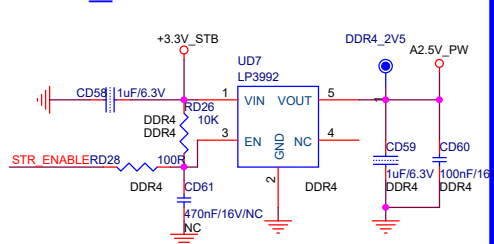
SW



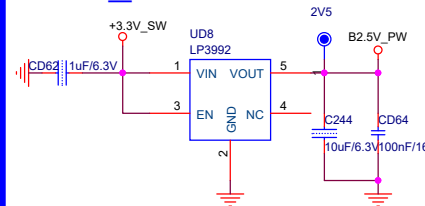
+5V_SW



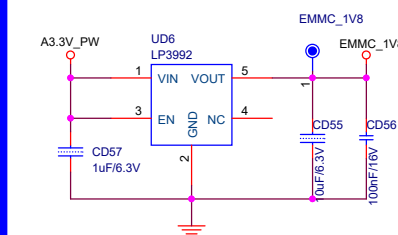
DDR4_2.5V



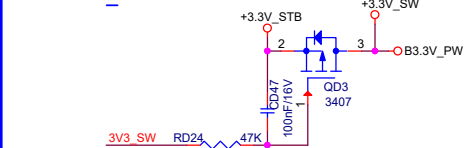
MAIN_2.5V



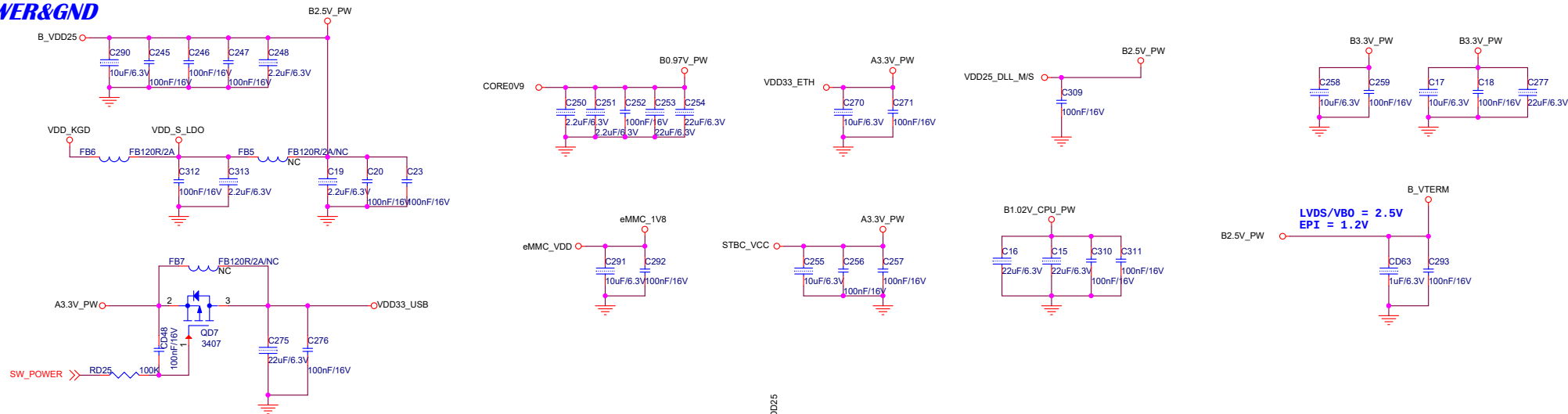
EMMC 1.8V



+3.3V_SW



IC POWER&GND

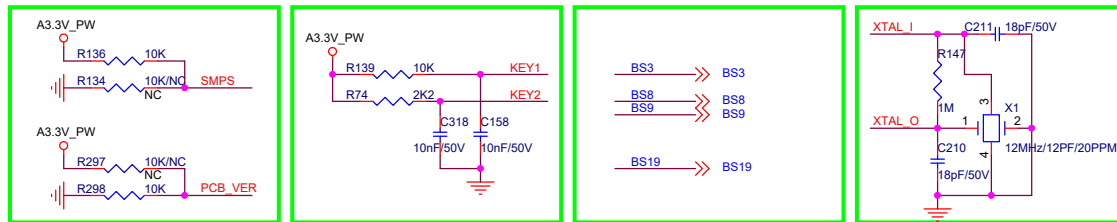
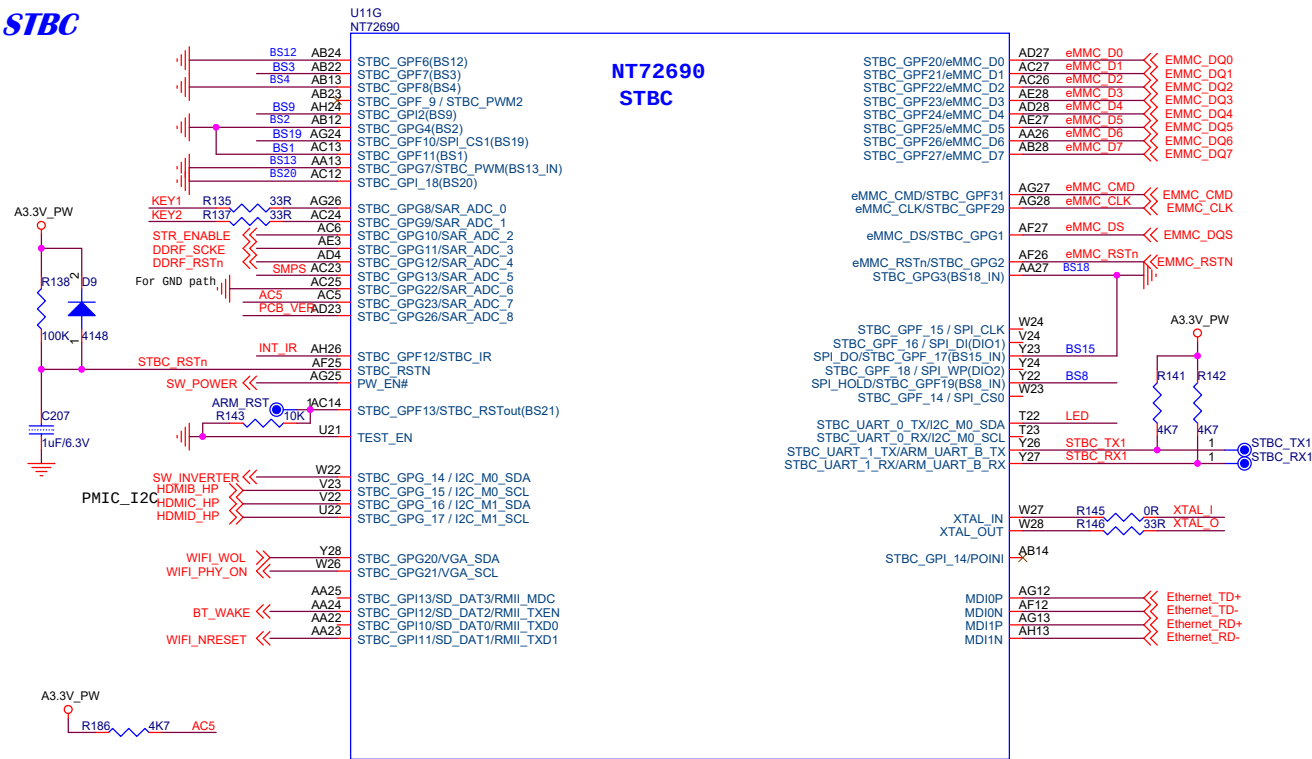


NT72690
POWER/GND

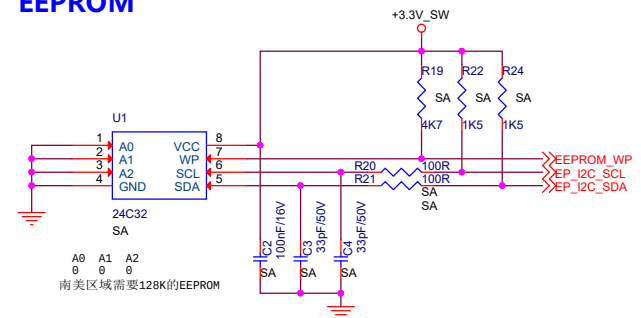
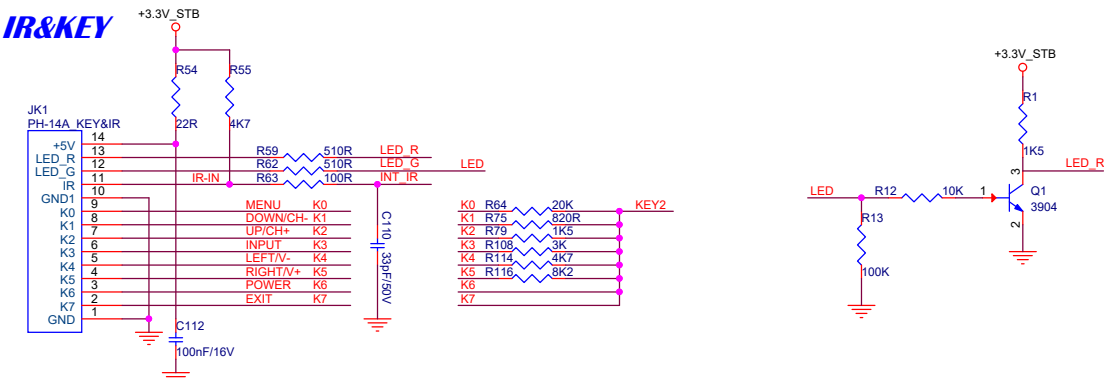
NAMING RULE
External Main side DDR4/DDR3
Sub side DDR4 KGD/DDR3 KGD

A1	GND	A14	GND	A27	GND
A2	GND	A15	GND	A28	GND
A3	GND	A16	GND	A29	GND
A4	GND	A17	GND	A30	GND
A5	GND	A18	GND	A31	GND
A6	GND	A19	GND	A32	GND
A7	GND	A20	GND	A33	GND
A8	GND	A21	GND	A34	GND
A9	GND	A22	GND	A35	GND
A10	GND	A23	GND	A36	GND
A11	GND	A24	GND	A37	GND
A12	GND	A25	GND	A38	GND
A13	GND	A26	GND	A39	GND
A14	GND	A27	GND	A40	GND
A15	GND	A28	GND	A41	GND
A16	GND	A29	GND	A42	GND
A17	GND	A30	GND	A43	GND
A18	GND	A31	GND	A44	GND
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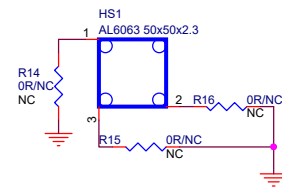
STBC

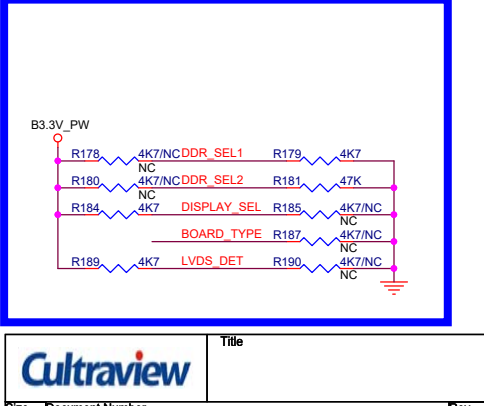
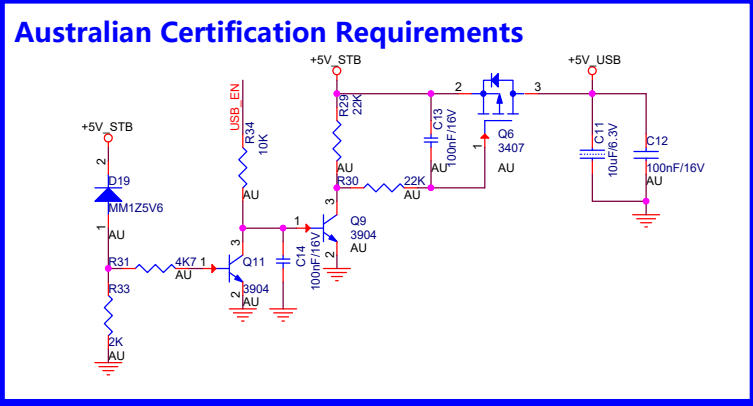
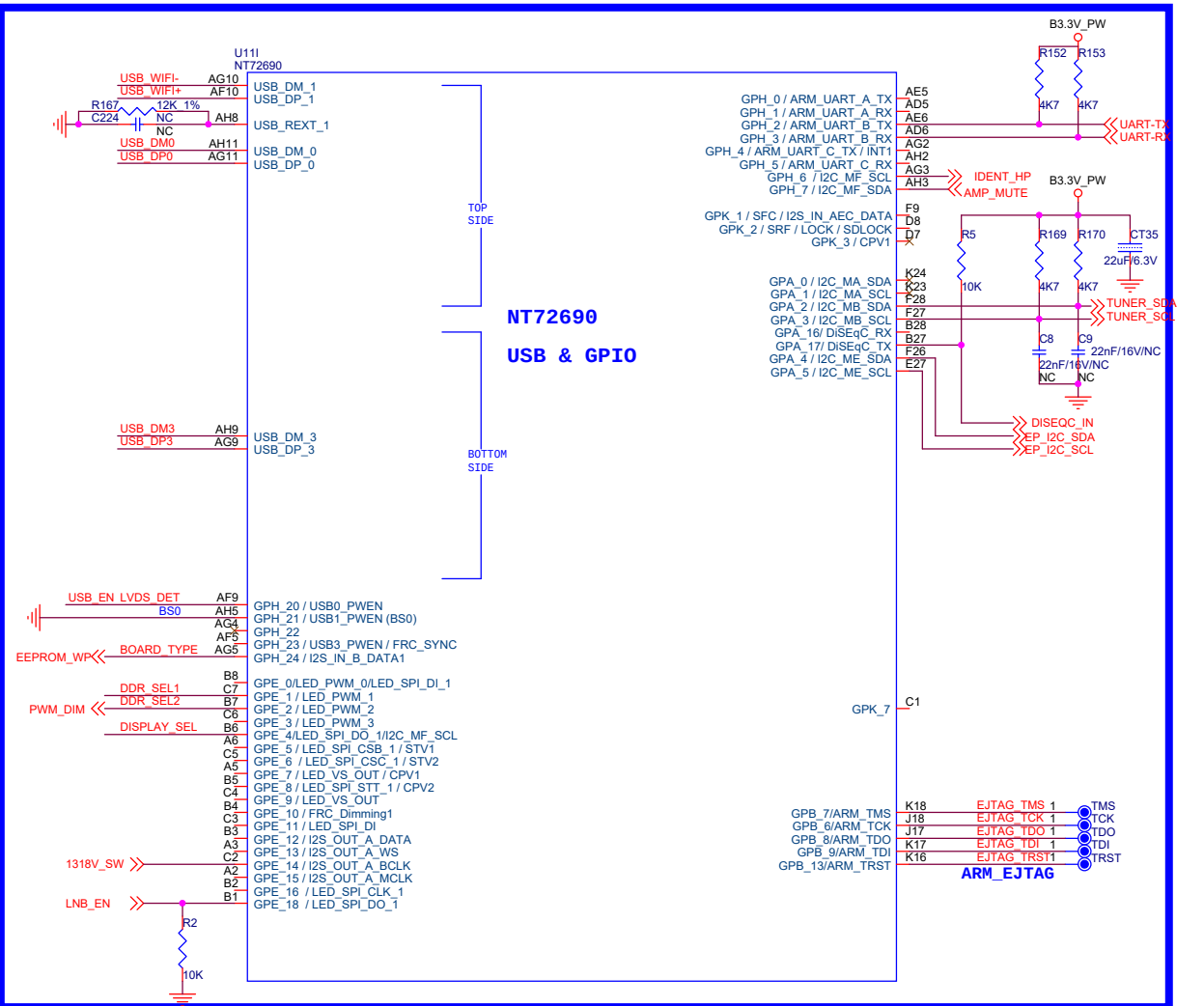
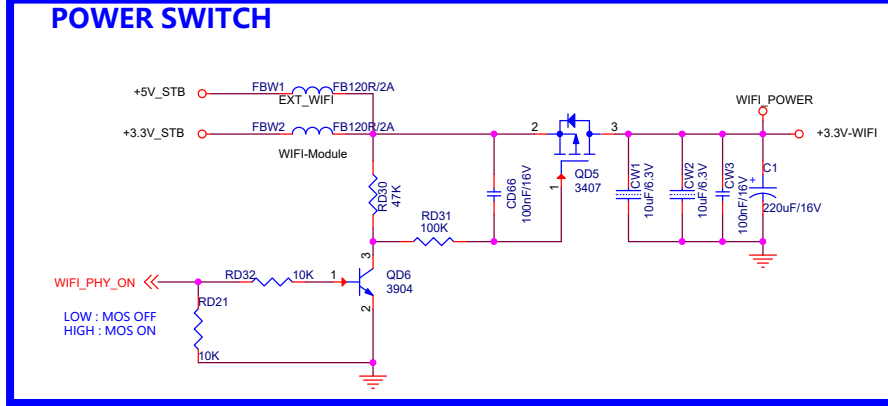
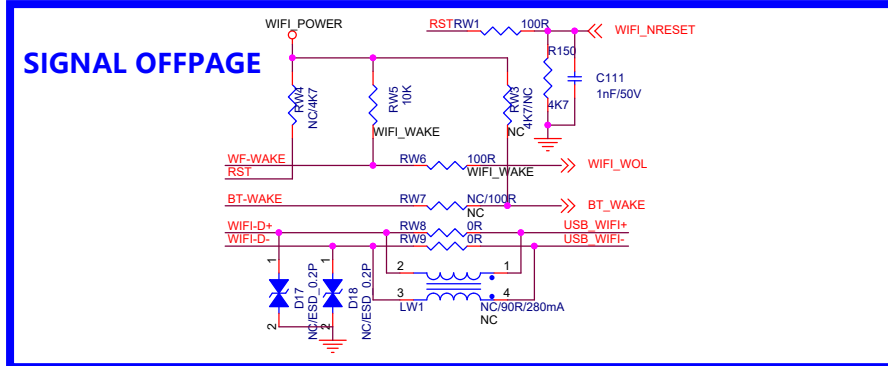
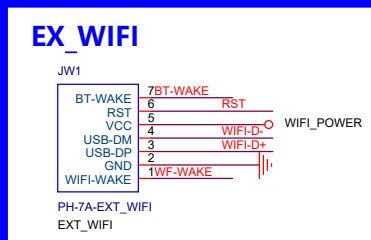
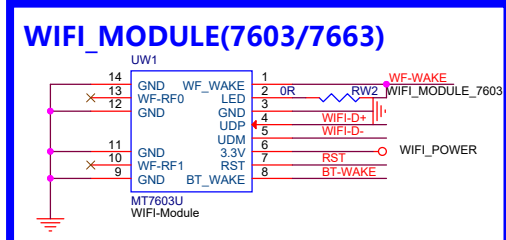
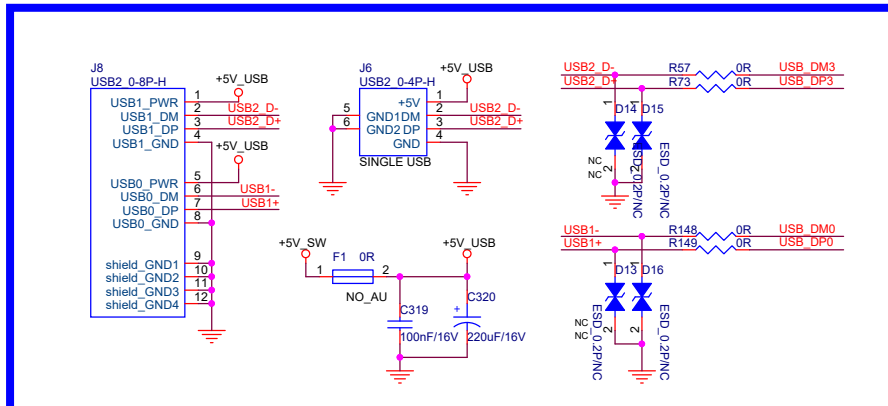


EEPROM

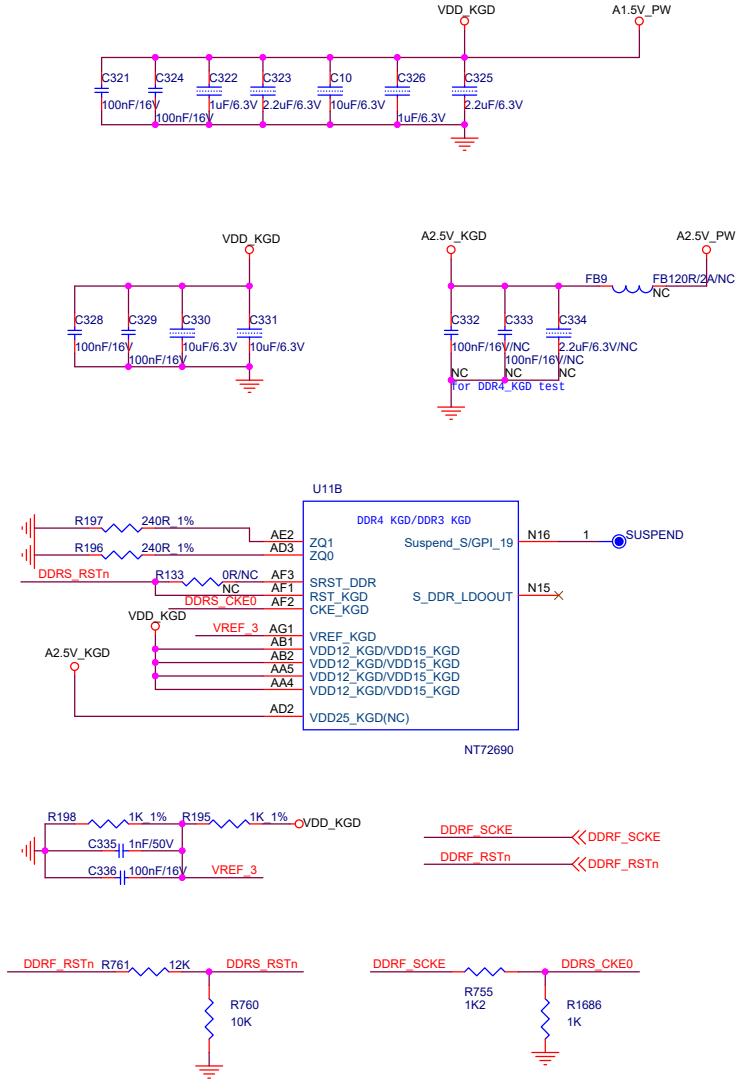
**IR&KEY**

Heat Sink

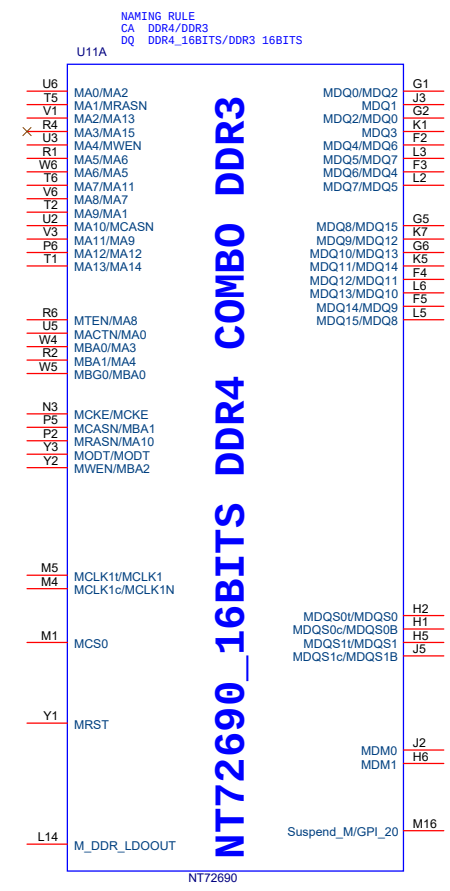




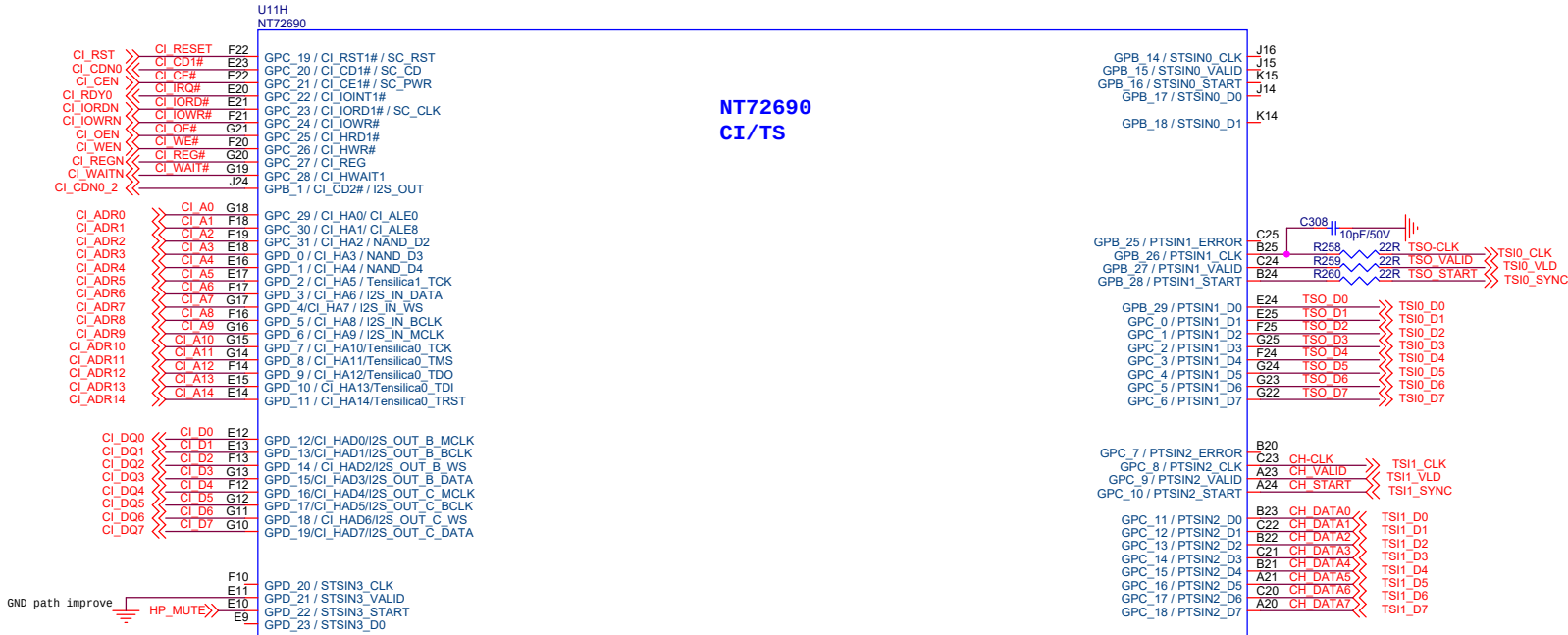
DDR_S



DDR_M



NT72690 CI/TS



CPU Side:

BS0_Bypass CPU MaskROM

0 : Using CPU MaskROM
1 : Bypass CPU MaskROM

STBC Side:

BS1_STBC Boot Strap Option

0: Boot from STBC
1: Boot from CPU, bypass STBC.

BS8_STBC watchdog

0: Default disable STBC watchdog
1: Default enable STBC watchdog

BS19_Internal boot strap for NF/eMMC type

0: NF/eMMC type internal boot strap enable
1: NF/eMMC type internal boot strap disable
(BS[7:6] = 00, BS8 is external; BS[17:16]=00,BS14=0, BS13,BS15,BS18 are external)

BS2_Bypass STBC MaskROM

When BS1=0,
0: Through STBC MaskROM
1: Bypass STBC MaskROM

BS12=0 , BS3,BS4_Device

BS4, 3 =
00: STBC boot from SPI, CPU boot from eMMC
01: STBC & CPU both boot from eMMC
10: STBC & CPU both boot from SPI
11: Reserved (same 00)

eMMC:

BS13_eMMC bus width

BS13 =
0: EMMC Bus width is 8 bit
1: EMMC Bus width is 4 bit

BS15_eMMC ACK

0: Boot mode wait ACK
1: Boot mode do not wait ACK

BS18_eMMC clk_switch

0: 26M
1: 13M

BS9_Security boot

0: no security boot
1: security boot

BS20_NAND I/O

0: NAND I/O in STBC eMMC side (BS12 = 1)
1: NAND I/O in ARM CI side (BS12 = 1, BS[4:3] = 00, 11)
or STBC SPI side (BS12 = 1, BS[4:3] = 01, 10)

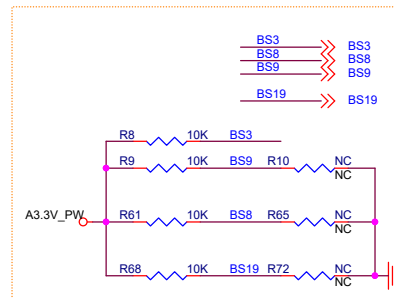
BS10_SPI Flash scramble

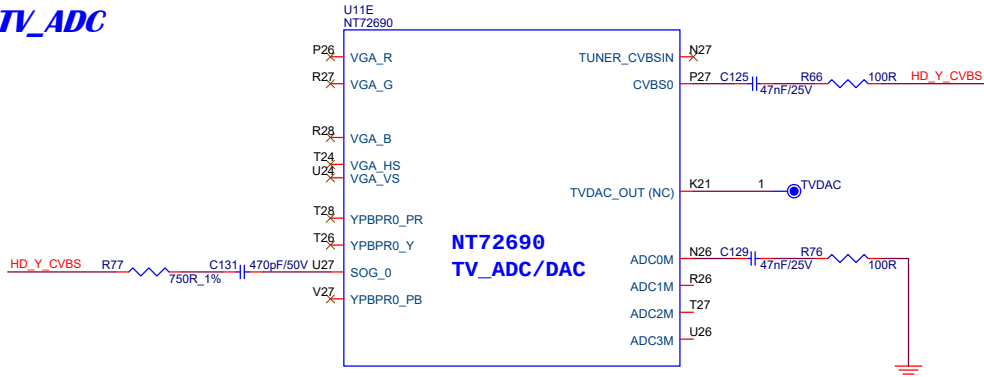
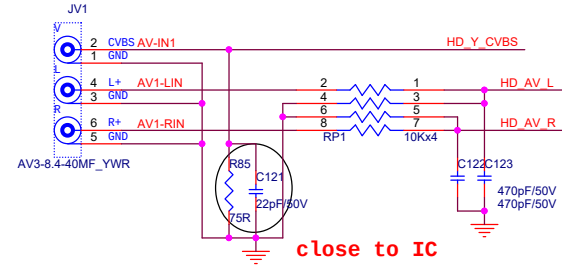
0: Disable
1: Enable

BS11_Turnkey Security

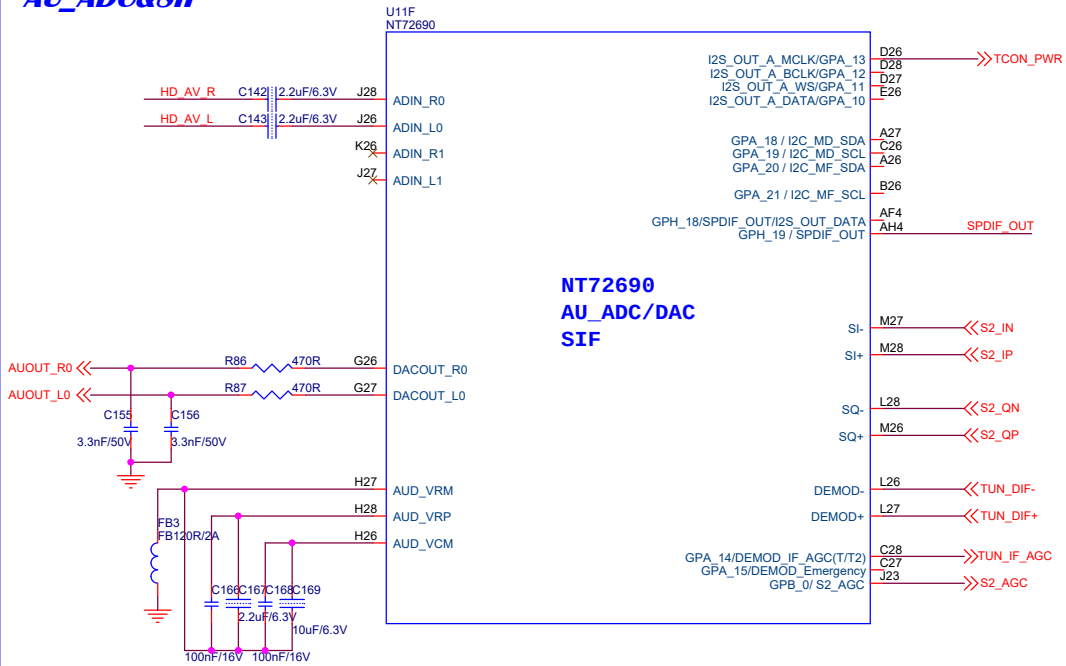
0: Disable
1: Enable

Internal
Bootstrap

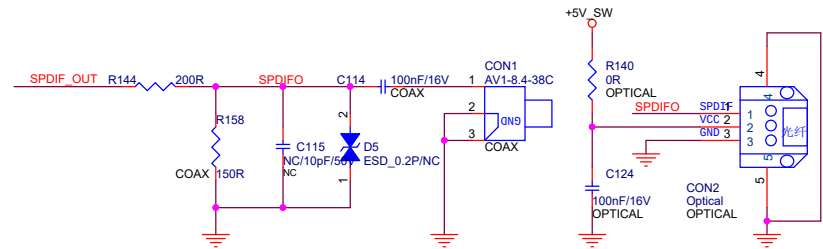


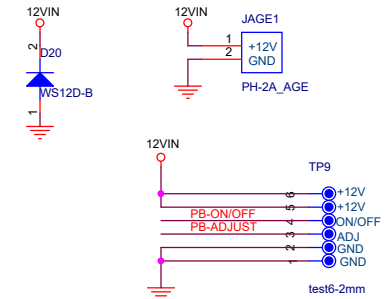
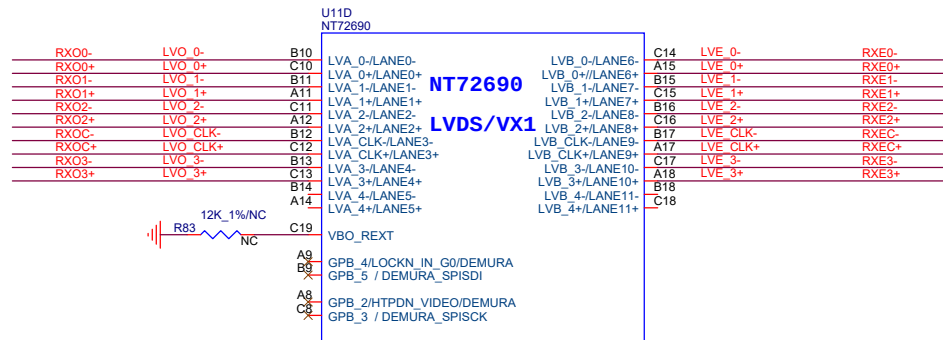
TV_ADC**AV1_IN**

AU_ADC&SIF

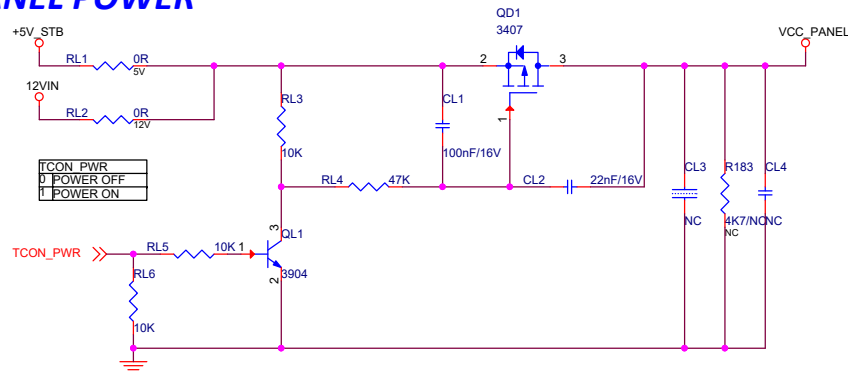


SPDIF OUT

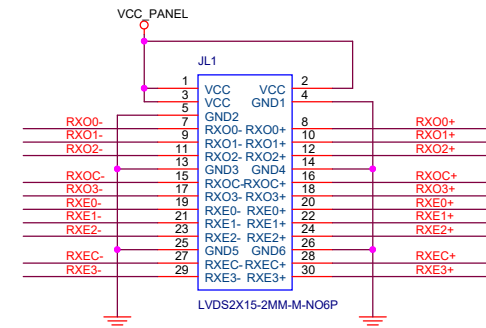




PANEL POWER



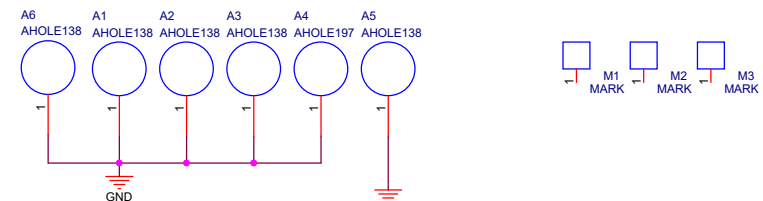
LVDS



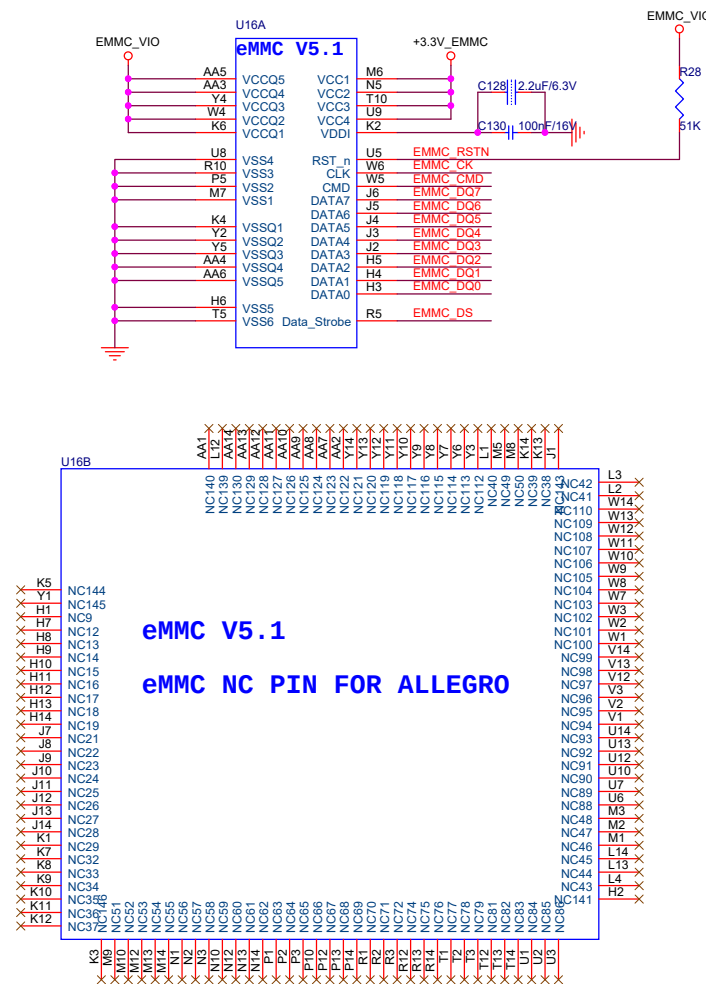
BackLight Controler



MARK & HOLE

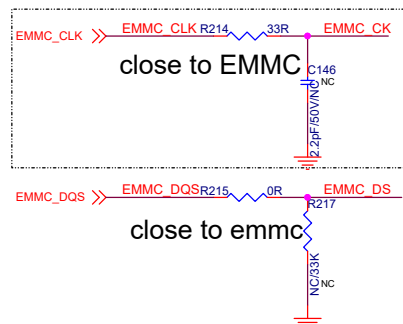


EMMC

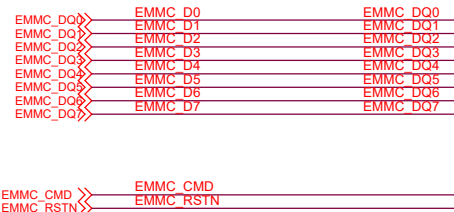


EMMC V5.1

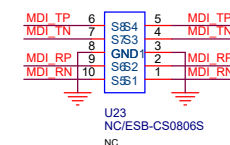
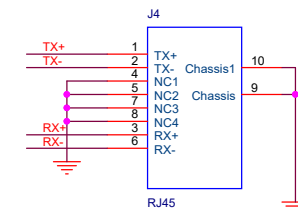
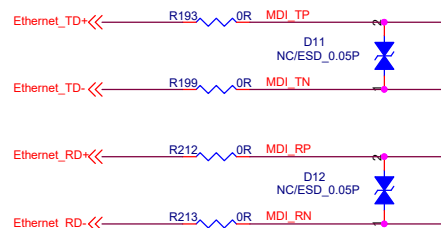
EMMC NC PIN FOR ALLEGRO



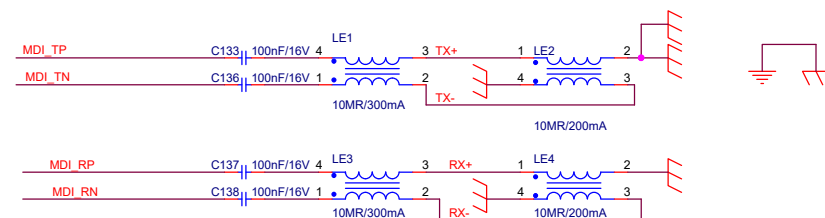
EMMC NET



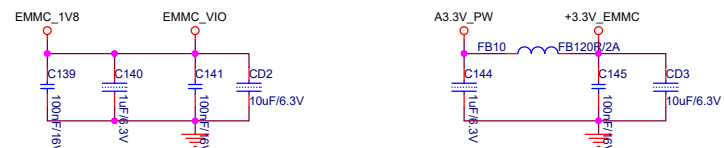
Ethernet Connetor



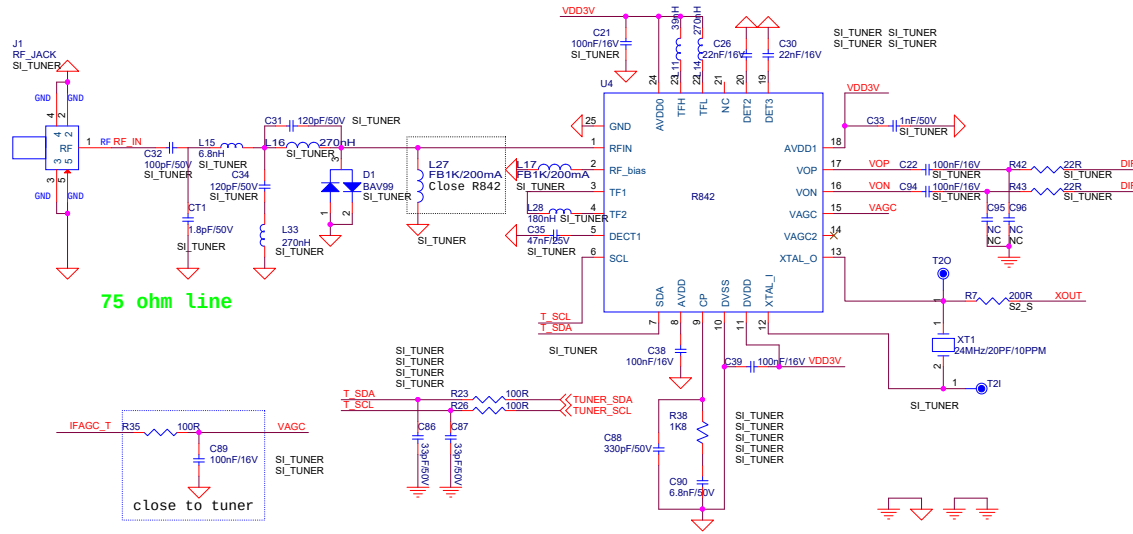
ENTHERNET 分立



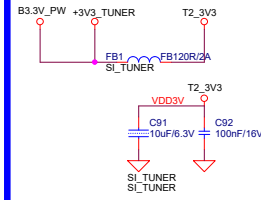
EMMC Power



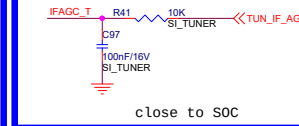
T/T2/C TUNER



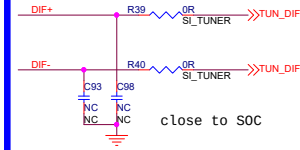
T2 Tuner Power



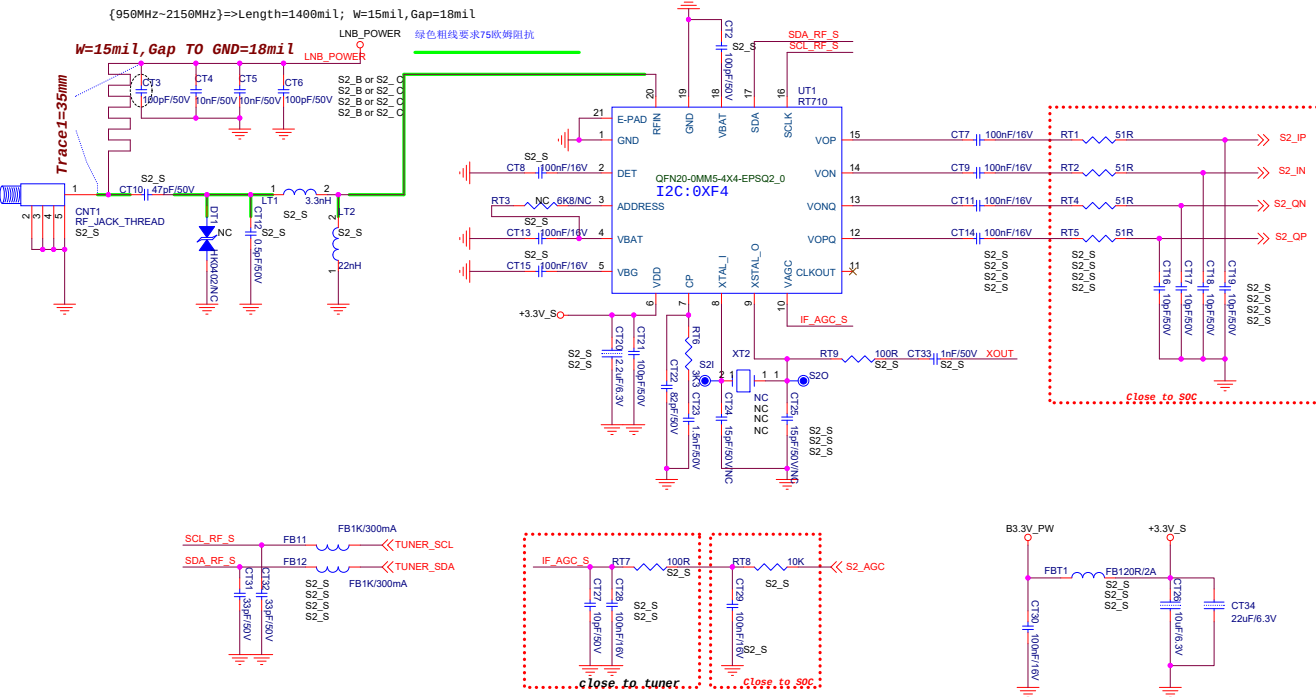
T2_AGC



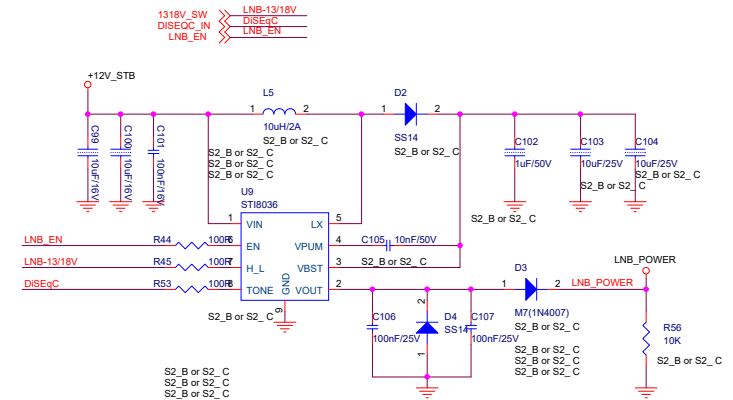
T2_IF



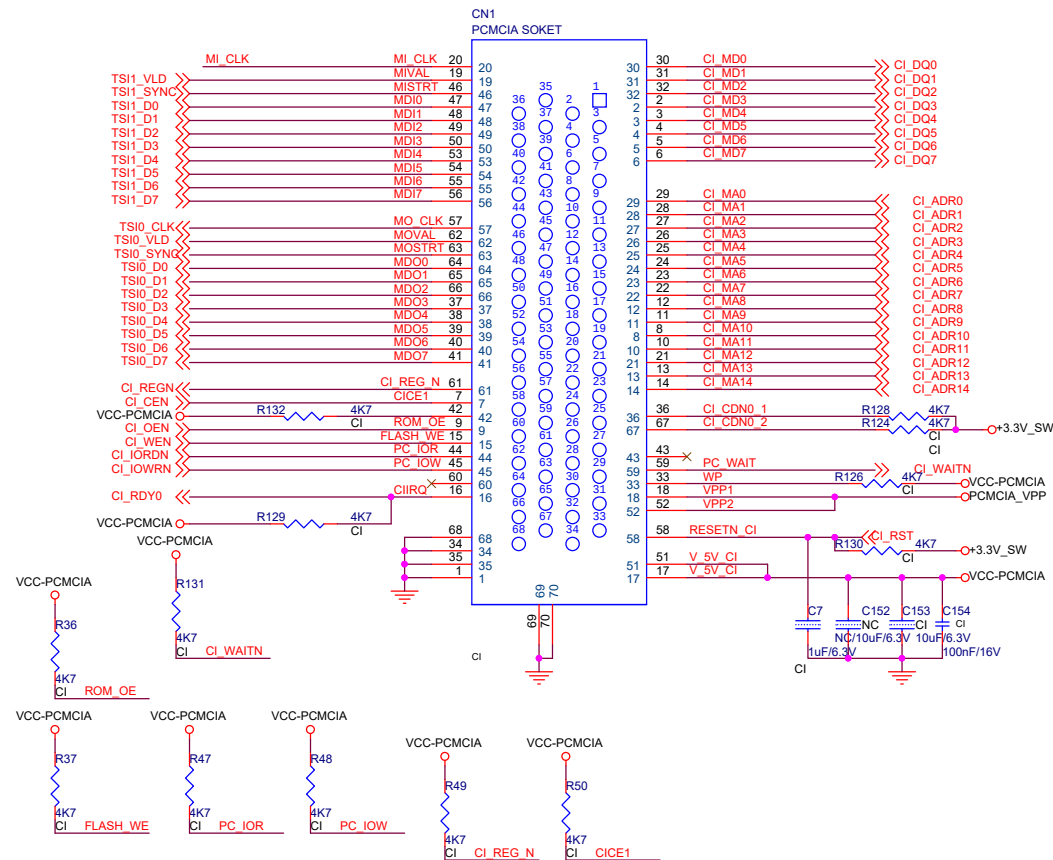
S2 TUNER



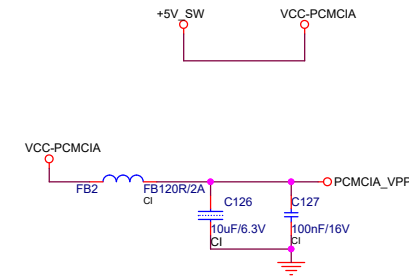
LNB POWER



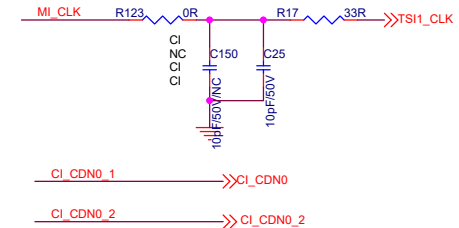
CI Socket



PCMCIA POWER



CLK



Headphone OP

The schematic diagram illustrates the Headphone OP circuit. The central component is the U2 (APA2172AOI-TRG) op-amp. The circuit includes several input and output stages, a voltage divider for a 3.3V output, and a feedback network. Key components and connections are as follows:

- Inputs:**
 - AMP_RIN: Connected to pin 2 via CA29 (2.2uF/6.3V) and RA14 (16K_1%).
 - AMP_REF: Connected to pin 1.
 - AMP_LIN: Connected to pin 14 via CA30 (2.2uF/6.3V) and RA17 (16K_1%).
 - HP_EN: Connected to pin 5.
- Outputs:**
 - EAR_ROUT: Connected to pin 3 via RA15 (68R).
 - EAR_LOUT: Connected to pin 13 via RA16 (68R).
 - 3.3V_SW: Connected to pin 11 via FB4 (FB120R/2A) and CA36 (10uF/6.3V).
- Internal Connections:**
 - Pin 12 is connected to pin 11 via RA18 (15K_1%) and CA31 (100nF/16V/NC).
 - Pin 9 is connected to pin 11 via UVPRA6 (30K_1%).
 - Pin 8 is connected to pin 7 via CPP.
 - Pin 7 is connected to pin 11 via RA21 (100K_1%) and CA32 (1uF/6.3V).
 - Pin 4 is connected to pin 10 via CA33 (150pF/50V/NC).
 - Pin 10 is connected to pin 11 via CA34 (1uF/6.3V).
 - Pin 11 is connected to pin 12 via CA35 (100nF/16V).
- Power and Grounding:**
 - VDD (pin 9) and VSS (pin 8) are connected to a common ground.
 - SDN (pin 5) and PGND (pin 10) are connected to a common ground.
 - GND (pin 4) is connected to a common ground.

POWER

The diagram illustrates the power supply for the CA24 module. A red wire connects the +12V_STB and AMP_POWER pins to a central node labeled PVDD. A blue capacitor, labeled CA24 470uF/16V, is connected between PVDD and GND.

MUTE

AMP_MUTE >>

RA10 4K7 AMP-EN

RA11

4K7

AMP_MUTE
0 MUTE
1 NORMAL

The diagram shows the MUTE pin configuration. A red wire labeled AMP_MUTE >> is connected to the MUTE pin. This wire passes through a 4K7 resistor (RA10) to a red wire labeled AMP-EN. The MUTE pin is also connected to a 4K7 resistor (RA11) which is connected to ground.

[illegible]

