MODEL No. DB645E23LH0

DEVICE SPECIFICATION

FOR

TFT-LCD Open Cell

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1. GENERAL DESCRIPTION

The specification is applied to 64.5" model (DB645E23LH0) TFT Liquid Crystal Display open cell and it supports 3840*2160 UD mode with 16.7M color depth (8bit) . This product is with data driver ICs and two 96-pins connectors with Mini-LVDS interface on each left1;2 and right1;2 4X-PCBA without built-in backlight unit.

1.1 General Specifications

Item	Specification	Unit	Note
Screen Size	64.5 inch Diagonal	-	-
Outline Dimension	1438.48 (H) ×856.66(V) x3.6(D)	mm	
Active Area	1428.48 (H) ×803.52 (V)	mm	
Driver Element	a-si TFT active matrix	-	-
GOA Type	Yes	-	-
Pixel Number	3840×2160	pixel	-
Sub Pixel Pitch	0.372(H) × 0.372(V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	16.7M	Color Depth	8bit
Display Mode	Normally Black	-	-
Panel Inversion Type	Column inversion	-	-
Weight	3.4	Kg	-

Note :

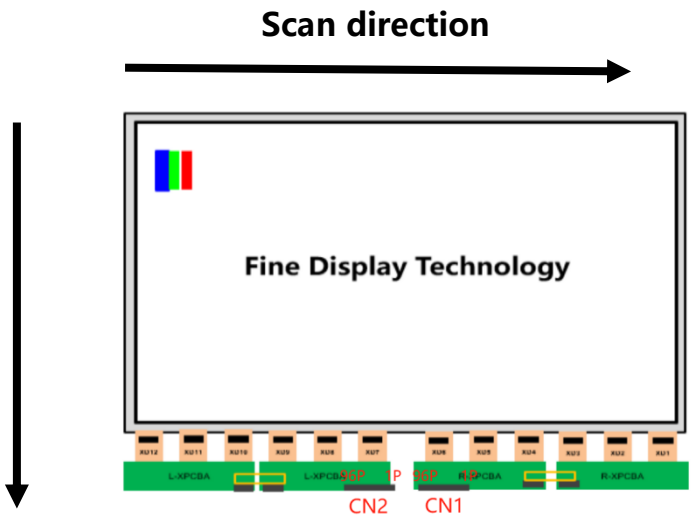


Fig 1.1 Display Orientation

2. ABSOLUTE MAXIMUM RATINGS

2.1 Absolute Maximun Ratings& Absolute Ratings of Environment

The followings are maximum values which, if exceeded, may cause damage to the unit. Temperature and relative humidity range is shown in the figure below.

Item	Symbol	Value		Unit	Note
		Min.	Max.		
VDD_3V3	VDD_3V3	-0.5	3.6	V	(1)
AVDD	AVDD	-0.5	18	V	(1)
Storage Temperature	TST	-20	60	°C	(2)
Operating Temperature	TOP	0	50	°C	(2), (3), (4)

Note:

(1) Within Ta=25±2°C

(2) a. 90 % RH Max. (Ta ≤ 40 °C)

b. Web-bulb temperature should be 39℃ Max. (Ta>40°C)

c. No condensation

d. Operating condition with a assemble module.

(3) The temperature of panel surface should be 0°C min. and 50°C max.

(4) Any point on the Driver surface must be less than 120°C under any condition. Module designer should apply adequate thermal solutions to keep the electrical components surface temperature under control limit (ex: Source Driver IC 120°C, Components on T-con PCB 100°C). Operation over the temperature can cause damages or decrease of life time.

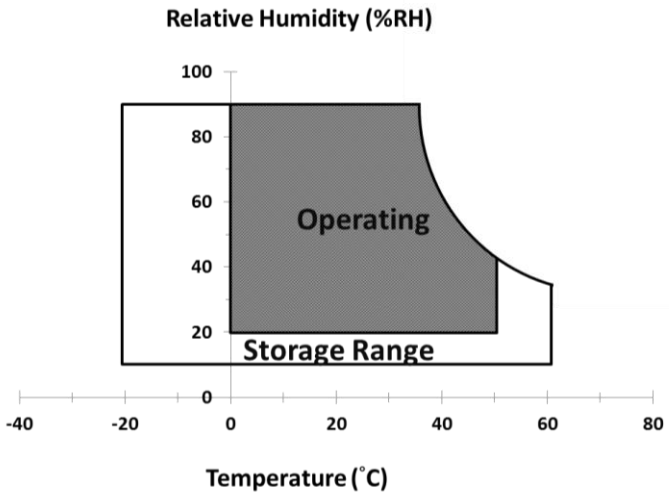


Fig.2.1 Operating and Storage Environment

3. ELECTRICAL SPECIFICATIONS

3.1 Electrical Characteristics

3.1.1 Power Consumption

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Analog power supply	AVDD	17.25	17.4	17.55	V	-
Analog power supply	HAVDD	8.28	8.43	8.58	V	-
Power supply for Gate on output	VGH (High level of CKV、STV)	34.5	35	35.5	V	
Power supply for Gate off output	VGL1	-6.5	-7	-7.5	V	-
Power supply for Common electrode	VCOM	7.6	7.75	7.9	V	(2)
Digital power supply	DCVDD3.3V	3.19	3.26	3.39	V	-
Gamma voltage	GAMMA1	16	16.2	16.3	V	-
	GAMMA2	14.85	15.1	15.2	V	-
	GAMMA3	12.75	12.85	12.95	V	-
	GAMMA4	11.75	12	12.1	V	-
	GAMMA5	11.15	11.3	11.45	V	-
	GAMMA6	11.09	11.19	11.29	V	-
	GAMMA7	8.83	8.93	9.03	V	-
	GAMMA8	7.94	8.04	8.15	V	-
	GAMMA9	5.52	5.67	5.82	V	-
	GAMMA10	5.41	5.51	5.62	V	-
	GAMMA11	4.69	4.79	4.89	V	
	GAMMA12	3.71	3.81	3.92	V	
	GAMMA13	1.25	1.38	1.48	V	
	GAMMA14	0.1	0.218	0.28	V	

Note:

(1) Ambient temperature: 25 ± 2°C;

(2) VCOM voltage depend on the flicker pattern’s performance; VCOM adjustable range: min ~ max value;

3.1.2 Power design current demand

Symbol	Max	Unit	Note
AVDD	3000	mA	-
HAVDD	80	mA	-
VGH	150	mA	-
VGL2	-	mA	-
VGL1	150	mA	-

VCOM	150	mA	-
DCVDD3.3V	500	mA	-
DCVDD1.2V	1000	mA	
DCVDD1.8V	300	mA	
GAMMA1	25	mA	-
GAMMA2	25	mA	-
GAMMA3	25	mA	-
GAMMA4	25	mA	-
GAMMA5	25	mA	-
GAMMA6	25	mA	-
GAMMA7	25	mA	-
GAMMA8	25	mA	
GAMMA9	25	mA	
GAMMA10	25	mA	
GAMMA11	25	mA	
GAMMA12	25	mA	-
GAMMA13	25	mA	-
GAMMA14	25	mA	-

3.1.3 Mini-LVDS Characteristics

Parameter	Symbol	Conditions	Min	Type	Max	Unit	Note
Mini-LVDS “L” input voltage	V_{ID}	3.0V≤VCC≤3.6V	150	-		mV	Note
Mini-LVDS input Voltage range	V_{RX}	-	GND	-	VCC	V	
Mini-LVDS common mode input voltage range	V_{COM}	3.0V≤VCC≤3.6V	-	1.2	1.4		

Note:

(1) Device will probably be damaged permanently in case that the stresses are over the absolute maximum ratings listed above.

(2) This VCC refers to the VCC(3.3V) of the driver part.

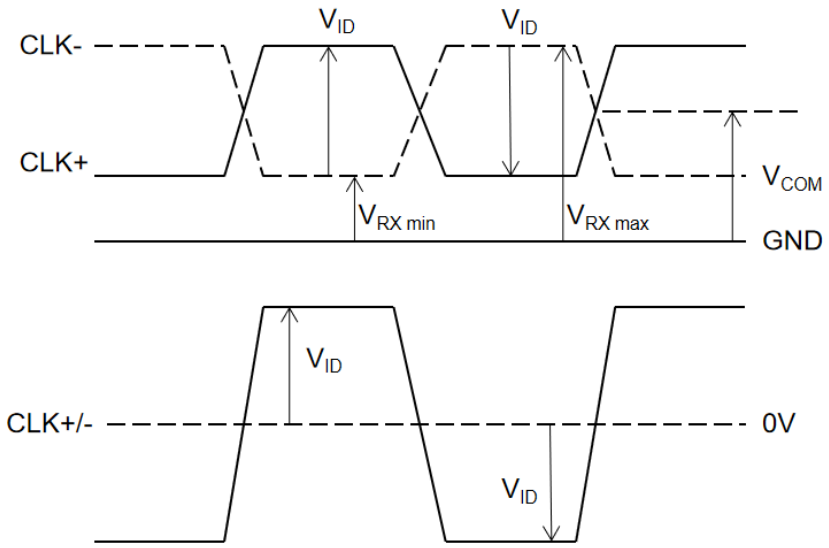


Fig 3.1.3 Mini-LVDS input signal

3.1.4 Mini-LVDS Eye Diagram

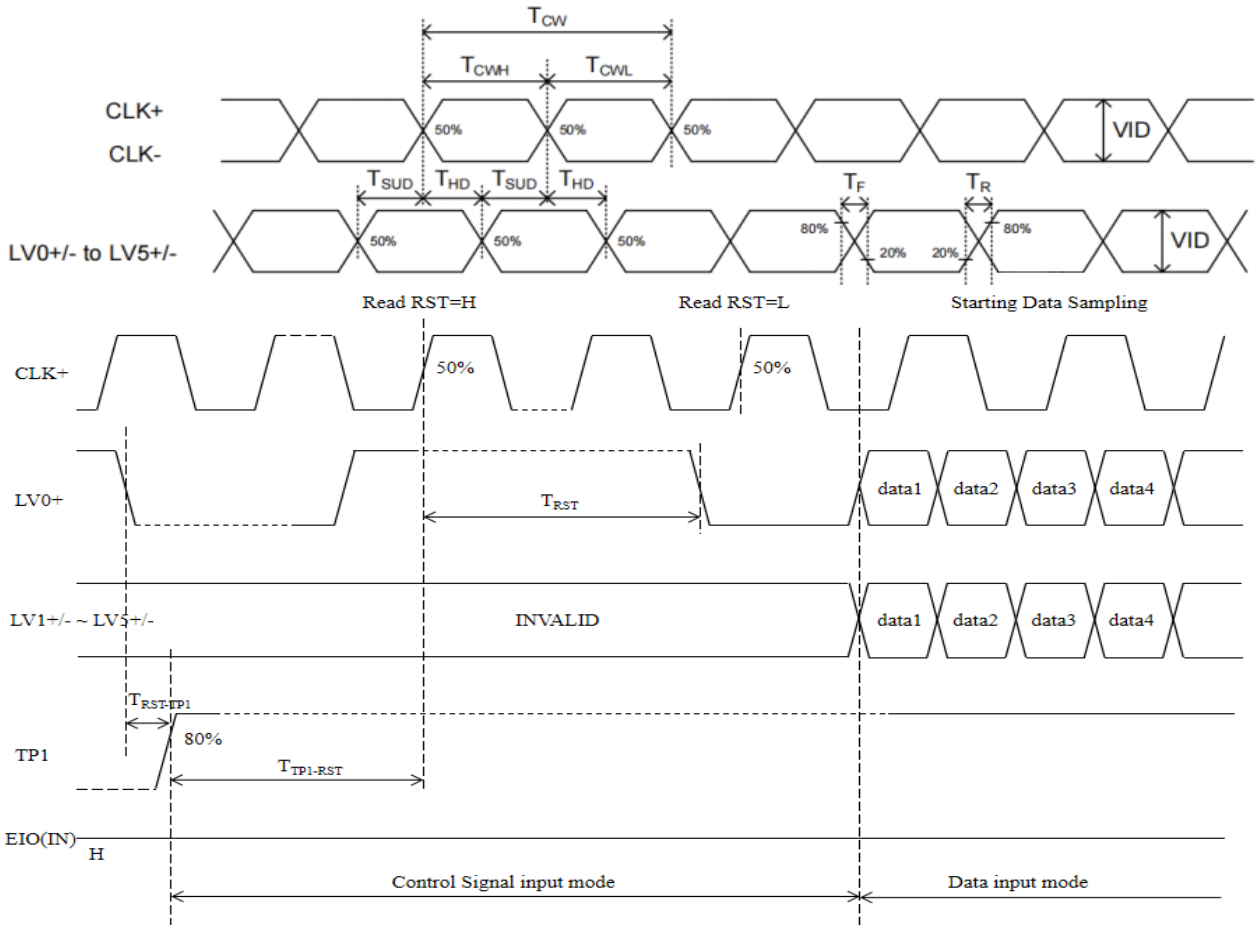


Fig 3.1.4 Mini-LVDS TP1-POL signal

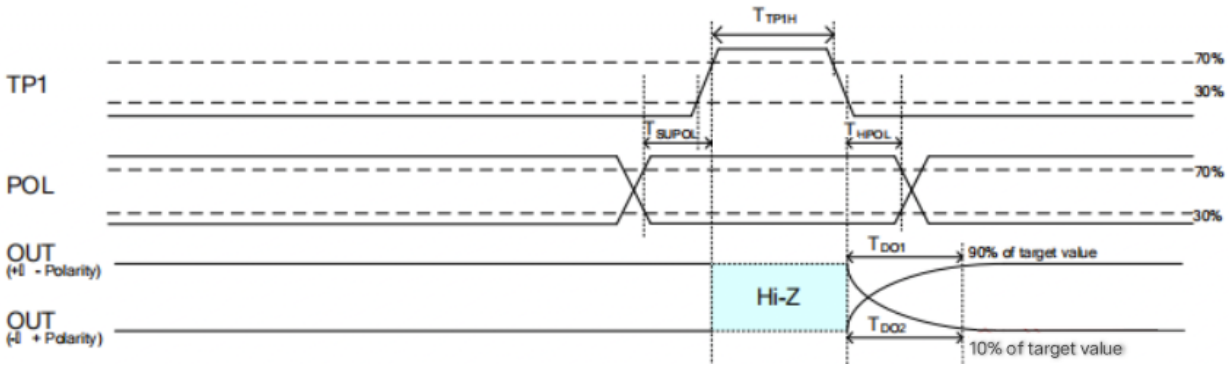


Table: Mini-LVDS Eye Diagram spec.

Parameter	Symbol	Spec				Note
		Min	Typ	Max	Unit	
Clock Period	T_{CW}	2.44	-	-	ns	
Clock high pulse width	T_{CWH}	0.4*CLK	-	0.6*CLK	ns	
Clock low pulse width	T_{CWL}	0.4*CLK	-	0.6*CLK	ns	
Data setup time	T_{SUD}	0.45	-	-	ns	
Data hold time	T_{HD}	0.45	-	-	ns	
CLK,LV[5:0] rising time	T_R	-	-	0.7	ns	
CLK,LV[5:0] falling time	T_F	-	-	0.7	ns	
Mini_RST(RESET) high	T_{RST}	3	-	-	CLK	Over 50ns
TP1 high period	T_{TP1H}	150	-	-	ns	
POL to TP1 setup time	T_{SUPOL}	5	-	-	ns	
TP1 to POL hold time	T_{HPOL}	250	-	-	ns	
Receiver off to TP1	T_{RO-TP1}	15	-	-	CLK	
TP1 to reset input time	$T_{TP1-RST}$	100	-	-	ns	
Reset low to TP1 input	$T_{RST-TP1}$	0	-	-	ns	

3.2 Interface Connections

3.2.1 Interface Pin Assignment

The input connect is JONHON FPC 21EJ0-105-0002_01 H=1.55 96P SMD or the same specification of other vender.

XL(CN2)			XR(CN1)		
N	Symbol	Description	No	Symbol	Description
1	GND	GND	1	GND	GND
2	NC	NC	2	NC	NC
3	NC	NC	3	NC	NC
4	NC	NC	4	VCOM	VCOM voltage
5	NC	NC	5	VCOM	VCOM voltage
6	GND	GND	6	NC	NC
7	NC	NC	7	AVDD	AVDD voltage
8	LS-VSS1	Power supply for GOA circuit	8	AVDD	AVDD voltage
9	LS-VSS1	Power supply for GOA circuit	9	AVDD	AVDD voltage
10	NC	NC	10	AVDD	AVDD voltage
11	LS-STV	STV input for GOA circuit	11	NC	NC

12	NC	NC	12	VCC33	DCVDD3.3V voltage
13	NC	NC	13	VCC33	DCVDD3.3V voltage
14	LS-CLK1	Clock input for GDL circuit	14	GND	GND
15	LS-CLK2	Clock input for GDL circuit	15	GAMMA14	GAMMA14 voltage
16	LS-CLK3	Clock input for GDL circuit	16	GAMMA13	GAMMA13 voltage
17	LS-CLK4	Clock input for GDL circuit	17	GAMMA12	GAMMA12 voltage
18	LS-CLK5	Clock input for GDL circuit	18	GAMMA11	GAMMA11 voltage
19	LS-CLK6	Clock input for GDL circuit	19	GAMMA10	GAMMA10 voltage
20	LS-CLK7	Clock input for GDL circuit	20	GAMMA9	GAMMA9 voltage
21	LS-CLK8	Clock input for GDL circuit	21	GAMMA8	GAMMA8 voltage
22	NC	NC	22	HAVDD	HAVDD voltage
23	LS-CLR	RST input for GOA circuit	23	GAMMA7	GAMMA7 voltage
24	NC	NC	24	GAMMA6	GAMMA6 voltage
25	NC	NC	25	GAMMA5	GAMMA5 voltage
26	NC	NC	26	GAMMA4	GAMMA4 voltage
27	NC	NC	27	GAMMA3	GAMMA3 voltage
28	GND	GND	28	GAMMA2	GAMMA2 voltage
29	LV0P-1	mini-LVDS Signal A0+	29	GAMMA1	GAMMA1 voltage
30	LV0N-1	mini-LVDS Signal A0-	30	NC	NC
31	LV1P-1	mini-LVDS Signal A1+	31	GND	GND
32	LV1N-1	mini-LVDS Signal A1-	32	FS	FS control signal
33	LV2P-1	mini-LVDS Signal A2+	33	POL	POL control signal
34	LV2N-1	mini-LVDS Signal A2-	34	TP	TP control signal
35	GND	GND	35	GND	GND
36	CLKP-1	mini-LVDS CLK Signal A +	36	LV0P-3	mini-LVDS Signal C0+
37	CLKN-1	mini-LVDS CLK Signal A -	37	LV0P-3	mini-LVDS Signal C0-
38	GND	GND	38	LV1P-3	mini-LVDS Signal C1+
39	LV3P-1	mini-LVDS Signal A3+	39	LV1N-3	mini-LVDS Signal C1-
40	LV3N-1	mini-LVDS Signal A3-	40	LV2P-3	mini-LVDS Signal C2+
41	LV4P-1	mini-LVDS Signal A4+	41	LV2N-3	mini-LVDS Signal C2-
42	LV4N-1	mini-LVDS Signal A4-	42	GND	GND
43	LV5P-1	mini-LVDS Signal A5+	43	CLKP-3	mini-LVDS CLK Signal C+
44	LV5N-1	mini-LVDS Signal A5-	44	CLKN-3	mini-LVDS CLK Signal C -
45	GND	GND	45	GND	GND
46	LV0P-2	mini-LVDS Signal B0+	46	LV3P-3	mini-LVDS Signal C3+
47	LV0P-2	mini-LVDS Signal B0-	47	LV3N-3	mini-LVDS Signal C3-
48	LV1P-2	mini-LVDS Signal B1+	48	LV4P-3	mini-LVDS Signal C4+
49	LV1N-2	mini-LVDS Signal B1-	49	LV4N-3	mini-LVDS Signal C4-
50	LV2P-2	mini-LVDS Signal B2+	50	LV5P-3	mini-LVDS Signal C5+
51	LV2N-2	mini-LVDS Signal B2-	51	LV5N-3	mini-LVDS Signal C5-
52	GND	GND	52	GND	GND
53	CLKP-2	mini-LVDS CLK Signal B +	53	LV0P-4	mini-LVDS Signal D0+
54	CLKN-2	mini-LVDS CLK Signal B -	54	LV0P-4	mini-LVDS Signal D0-
55	GND	GND	55	LV1P-4	mini-LVDS Signal D1+
56	LV3P-2	mini-LVDS Signal B3+	56	LV1N-4	mini-LVDS Signal D1-
57	LV3N-2	mini-LVDS Signal B3-	57	LV2P-4	mini-LVDS Signal D2+
58	LV4P-2	mini-LVDS Signal B4+	58	LV2N-4	mini-LVDS Signal D2-

59	LV4N-2	mini-LVDS Signal B4-	59	GND	GND
60	LV5P-2	mini-LVDS Signal B5+	60	CLKP-4	mini-LVDS CLK Signal D+
61	LV5N-2	mini-LVDS Signal B5-	61	CLKN-4	mini-LVDS CLK Signal D -
62	GND	GND	62	GND	GND
63	TP	TP control signal	63	LV3N-4	mini-LVDS Signal D3+
64	POL	POL control signal	64	LV3N-4	mini-LVDS Signal D3-
65	FS	FS control signal	65	LV4P-4	mini-LVDS Signal D4+
66	GND	GND	66	LV4N-4	mini-LVDS Signal D4-
67	GAMMA14	GAMMA14 voltage	67	LV5P-4	mini-LVDS Signal D5+
68	GAMMA13	GAMMA13 voltage	68	LV5N-4	mini-LVDS Signal D5-
69	GAMMA12	GAMMA12 voltage	69	GND	GND
70	GAMMA11	GAMMA11 voltage	70	NC	NC
71	GAMMA10	GAMMA10 voltage	71	NC	NC
72	GAMMA9	GAMMA9 voltage	72	NC	NC
73	GAMMA8	GAMMA8 voltage	73	NC	NC
74	HAVDD	HAVDD voltage	74	LS-CLR	RST input for GOA circuit
75	GAMMA7	GAMMA7 voltage	75	NC	NC
76	GAMMA6	GAMMA6 voltage	76	LS-CLK8	Clock input for GDL circuit
77	GAMMA5	GAMMA5 voltage	77	LS-CLK7	Clock input for GDL circuit
78	GAMMA4	GAMMA4 voltage	78	LS-CLK6	Clock input for GDL circuit
79	GAMMA3	GAMMA3 voltage	79	LS-CLK5	Clock input for GDL circuit
80	GAMMA2	GAMMA2 voltage	80	LS-CLK4	Clock input for GDL circuit
81	GAMMA1	GAMMA1 voltage	81	LS-CLK3	Clock input for GDL circuit
82	NC	NC	82	LS-CLK2	Clock input for GDL circuit
83	GND	GND	83	LS-CLK1	Clock input for GDL circuit
84	VCC33	DCVDD3.3V voltage	84	NC	NC
85	VCC33	DCVDD3.3V voltage	85	NC	NC
86	NC	NC	86	LS-STV	STV input for GOA circuit
87	AVDD	AVDD voltage	87	NC	NC
88	AVDD	AVDD voltage	88	LS-VSS1	Power supply for GOA
89	AVDD	AVDD voltage	89	LS-VSS1	Power supply for GOA
90	AVDD	AVDD voltage	90	NC	NC
91	NC	NC	91	GND	GND
92	VCOM	VCOM voltage	92	DEMURA-	Demura Flash Chip Select
93	VCOM	VCOM voltage	93	DEMURA-SDI	Demura Flash data input
94	NC	NC	94	DEMURA-	Demura Flash data output
95	NC	NC	95	DEMURA-	Demura Flash Serial Clock
96	GND	GND	96	GND	GND

Note: Connector direction sketch map

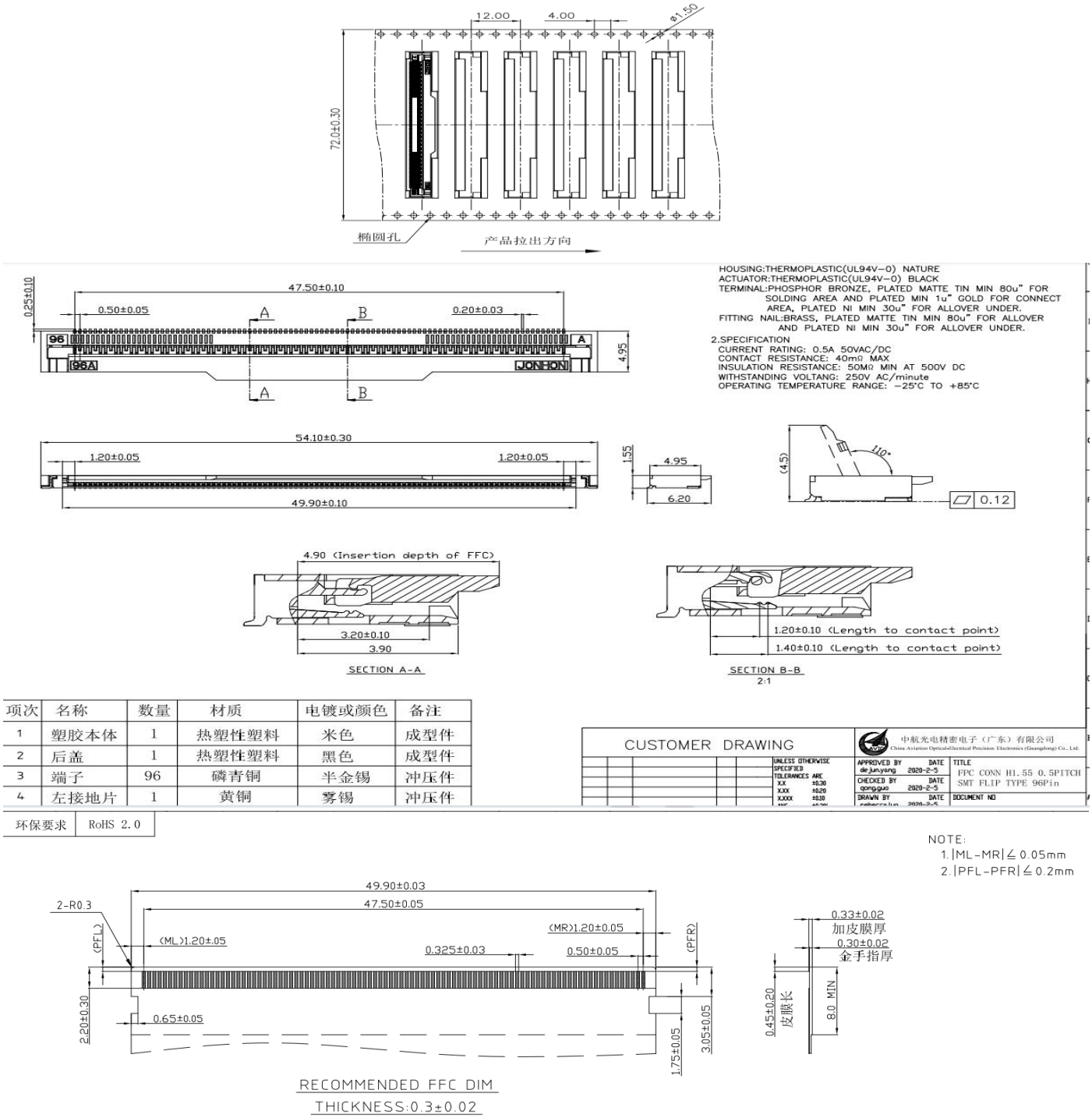
Left side CN2

Right side CN1

Fig 3.2.1 Mini-LVDS connector direction sketch map

3.2.2 Connector Drawing

Mini-LVDS Interface 96 Pin



项次	名称	数量	材质	电镀或颜色	备注
1	塑胶本体	1	热塑性塑料	米色	成型件
2	后盖	1	热塑性塑料	黑色	成型件
3	端子	96	磷青铜	半金锡	冲压件
4	左接地片	1	黄铜	雾锡	冲压件

环保要求	RoHS 2.0

Fig 3.2.2 Connector and FFC Drawing

3.3 Timing Spec

GDL Power on/off and Timing are as follows

TFT-LCD panel operating condition at 60Hz. (This panel is designed for 60Hz)

Table 3.3 shows the recommended condition to operate TFT-LCD panel.

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Main Gate voltage (high)	Vgh	-	35	-	V	
Main Gate voltage (low)	Vgl	-	-7	-	V	
Source voltage (high)	Vsh	-	16.2	-	V	[Note1]
Source voltage (low)	Vsl	-	0.2	-	V	[Note1]
Common voltage	Vcom	-	Adjustment	-	V	[Note2]
H total	1H	-	7.4	-	μs	
Gate ON-time	Ton	-	22.2	-	μs	
V total (1 frame)	1V	-	16.7	-	ms	60Hz

[Note1] The polarity of source signal must be inverted at every frame (included blanking period).

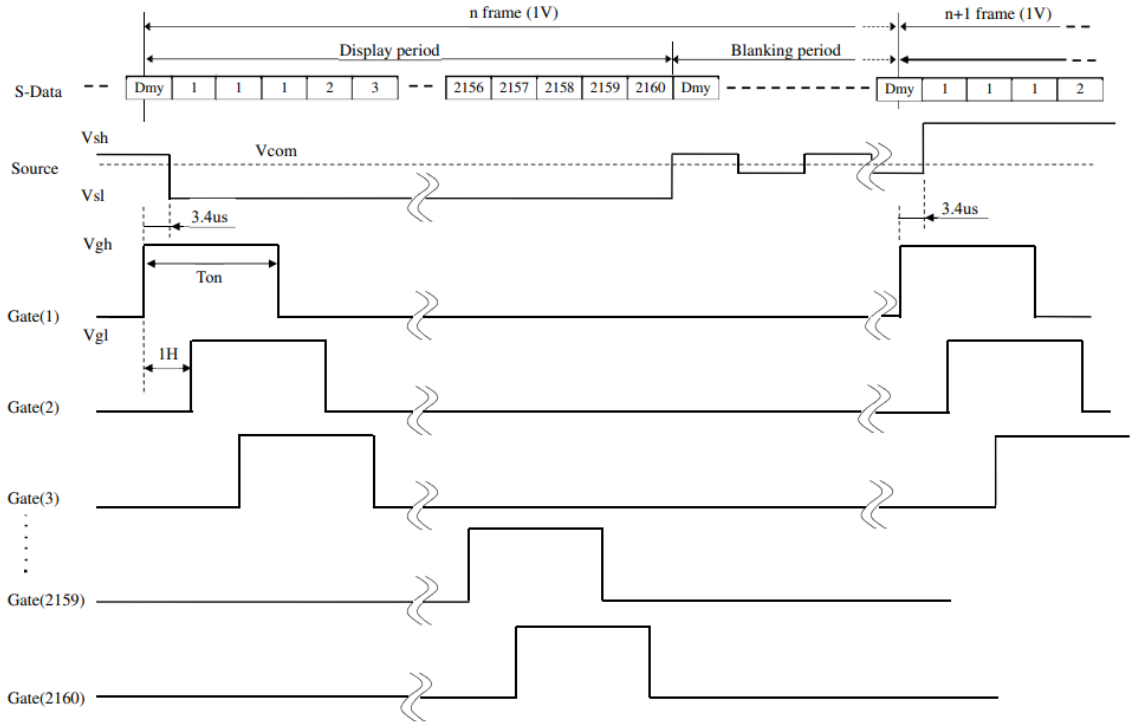


Fig.3.3-1: gate and source signal driving waveform.

[Note2] Common voltage must be adjusted at every panel. The adjustment pattern is shown as below.

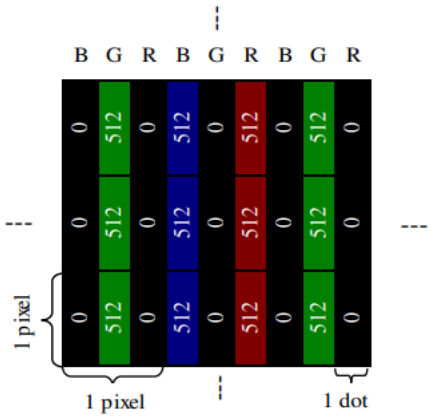


Fig.3.3-2: common voltage adjusting pattern:1-source-line-stripe.

(2) GOA signal timing (input)

Item	Symbol	Min	Typ.	Max.	unit	Remark
GSP_H	T_{GSPH}	-	4	-	H	
GCK_H	Ton	-	3	-	H	
GCK_L	Toff	-	5	-	H	
GCK_Shift	Td	-	1	-	H	
GEP_H	T_{GEPH}	-	4	-	H	
The end-line GCK↑to GEP↑	Tckgep	-	10	-	H	

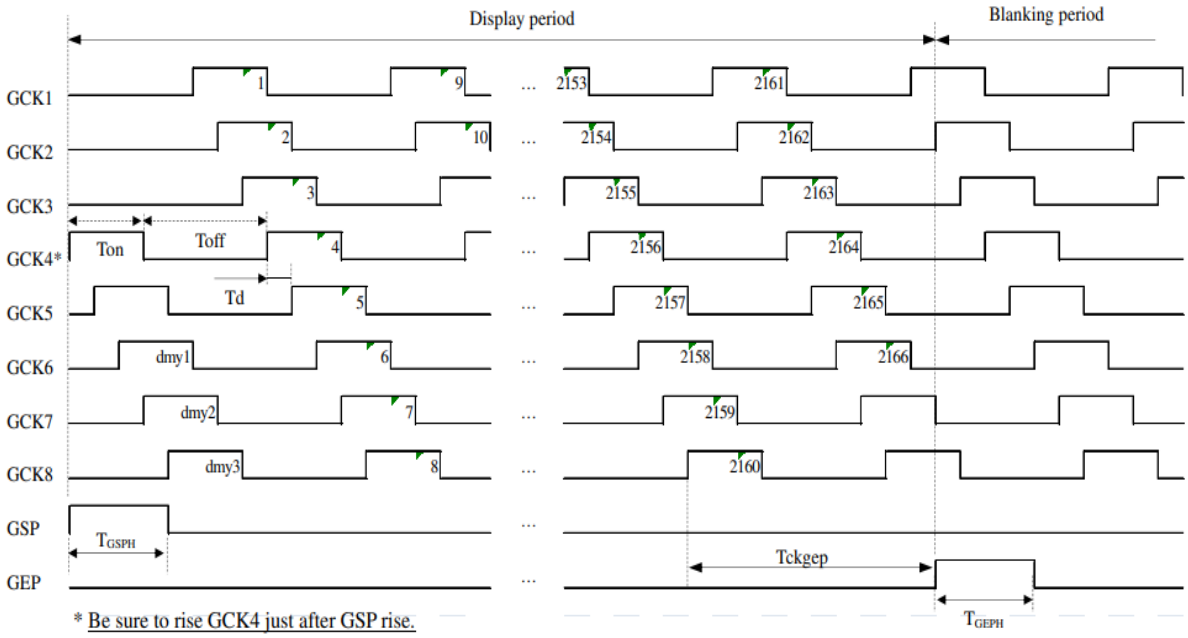


Fig.3.3-3: GOA signal timing(input).

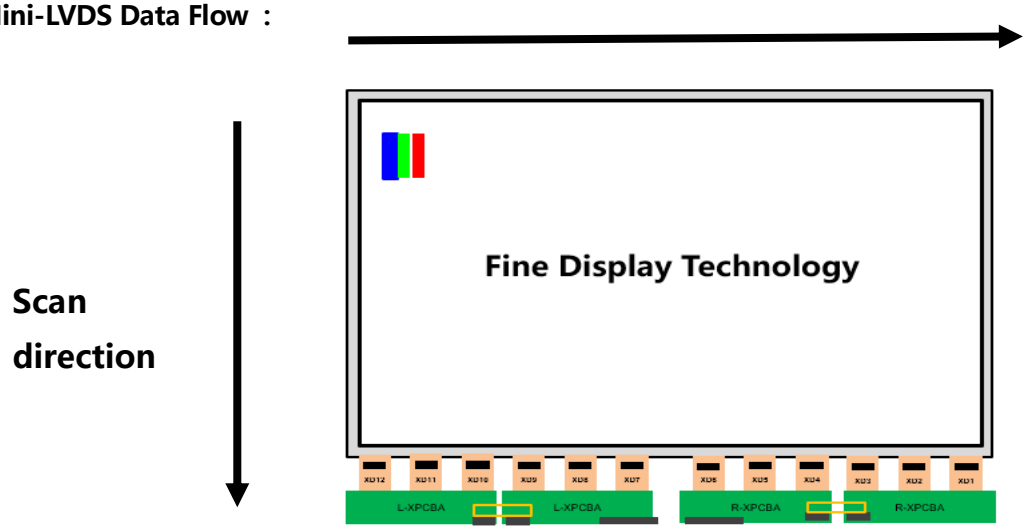
3.4 Mini-LVDS Data Mapping

Mini-LVDS information 60HZ/4port/6pair/8bit

Mini-LVDS data mapping:

R_LV[0..5]	**1**	**2**	**3**	**4**	**5**	**6**	**...**	**...**	**1915**	**1916**	**1917**	**1918**	**1919**	**1920**
L_LV[0..5]	**1921**	**1922**	**1923**	**1924**	**1925**	**1926**	**...**	**...**	**3835**	**3836**	**3837**	**3838**	**3839**	**3840**

Mini-LVDS Data Flow ：



Note: COF1~COF11 S-IC output channel will be 960CH; COF12 will be 961CH.

3.5 Power On/Off Sequence

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.

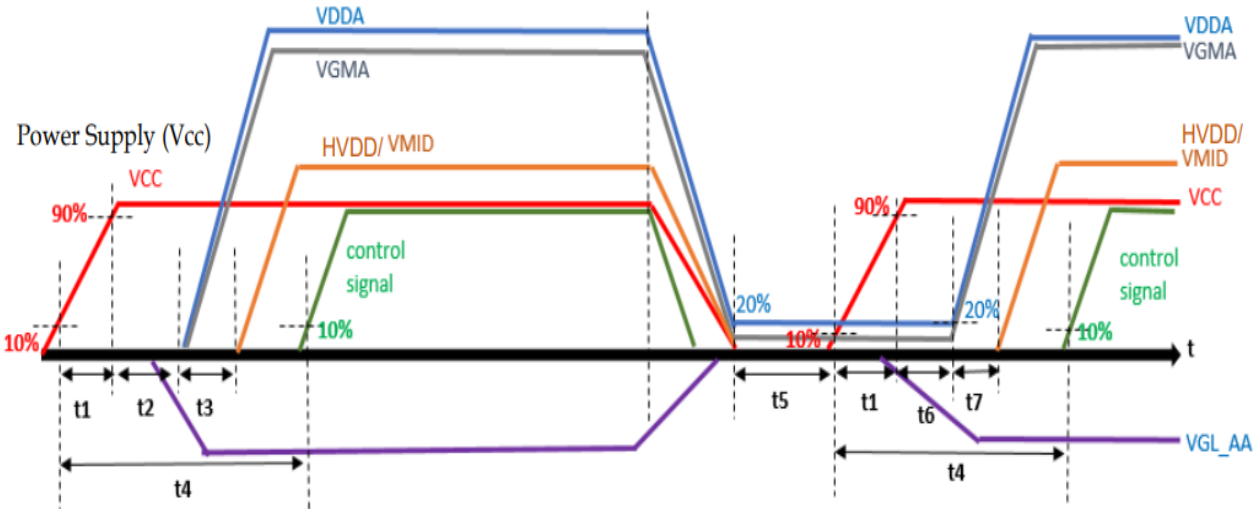


Fig 3.5 Power on/off

Parameters	Values			Units
	Min.	Typ.	Max.	
T1	0.5	-	10	ms
T2	0	-	-	ms
T3	0			
T4	0	-	-	ms
T5	0	-	-	ms
T6	0	-	-	ms
T7	0	-	-	ms

3.6 Flicker Adjustment

The polarity inversion mode is column inversion, and the diagram is as follows:

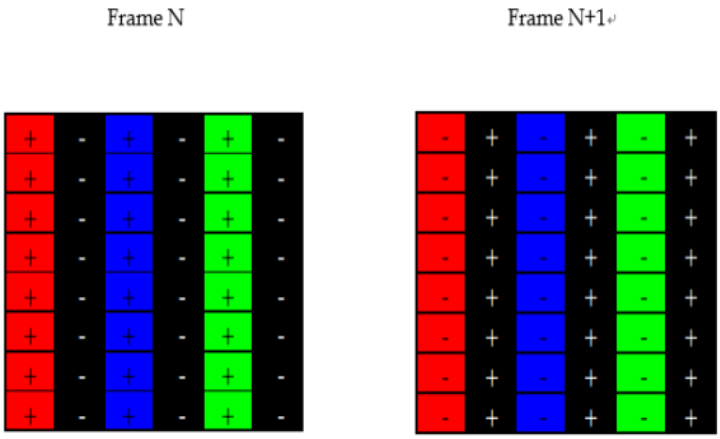


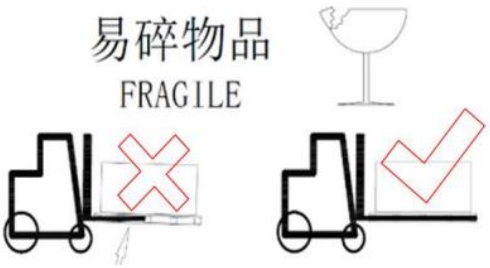
Fig 3.6 Column inversion flicker pattern diagram

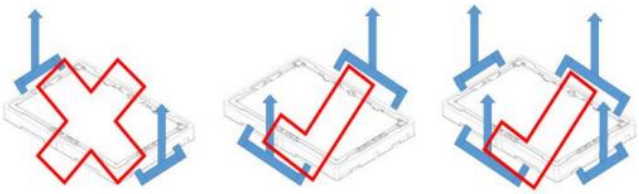
4. Packing

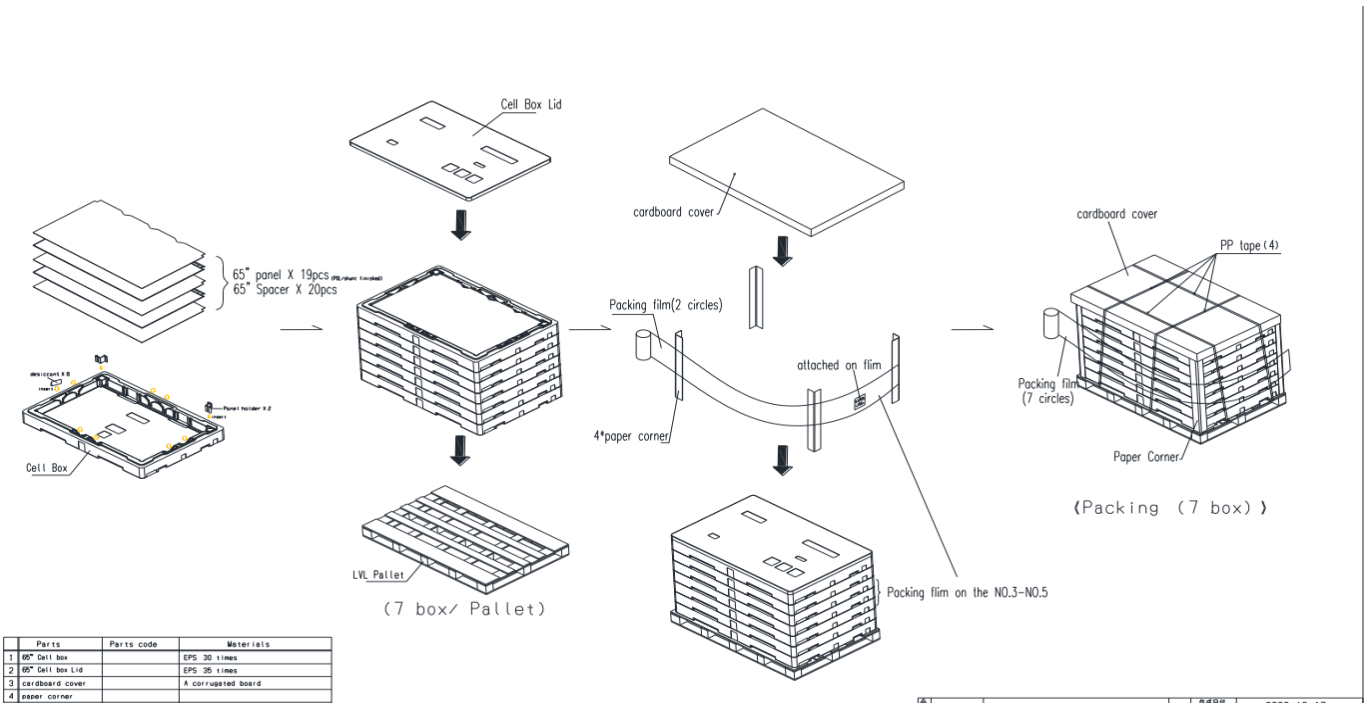
4.1 Packing Form

	1-pallet	1 box
size	1680x1110x1072 (H)[mm]	1640x1070x169[mm]
Q'ty	133 Open-Cells (7 boxes)	19 Open-Cells
Mass	About 530 Kg	About 73Kg

(1) 19 Pcs LCD Panels / 1 Box
(2) Box dimensions : 1640 (L) X 1070 (W) X 169 (H)mm
(3) Weight : approximately 73 Kg / 1 Box
(4) 133 PCS LCD TV Panels / 1 Pallet
(5) Group dimensions : 1680 (L) X 1110 (W) X1072 (H)mm
(6) Weight : approximately 530 Kg / 1 Pallet
(7) Please fill up the container to avoid any cargo be damaged.
(8) Recommend to follow the packing method as described in 10.2.
(9) When transferring in warehouse or factory, the arm length of electric forklift or hand pallet truck must be longer than the pallet. (Note 1)
(10) After un-packing, one box is needed to be carried on long edge which is to prevent box bent or fell down. (Note 2)
(11) The surface area of the worktable or carts should be greater than box size.



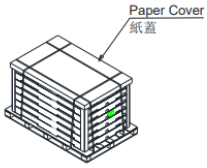




	Parts	Parts code	Materials
1	65" Cell box		EPS 30 times
2	65" Cell box Lid		EPS 35 times
3	cardboard cover		A corrugated board
4	paper corner		

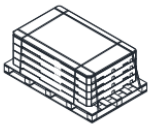
A TYPE
(Air transportion /single pallet with film)

Full



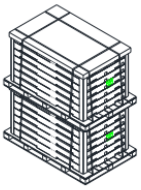
7 Boxes / Pallet

Not Full



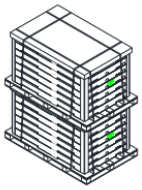
B TYPE
(Pile the upper pallet on the lower one)

Sea&Land Transportation
(40ft HQ Container)



7 Boxes / Pallet + 7 Boxes / Pallet

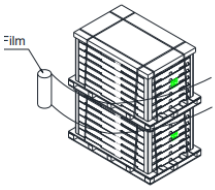
Sea&Land Transportation
(40ft Container)



7 Boxes / Pallet + 7 Boxes / Pallet

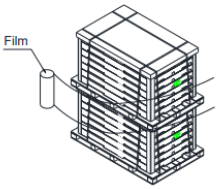
C TYPE (Two pallets with film)

Sea&Land Transportation
(40ft HQ Container)



7 Boxes / Pallet + 7 Boxes / Pallet

Sea&Land Transportation
(40ft Container)



7 Boxes / Pallet + 7 Boxes / Pallet

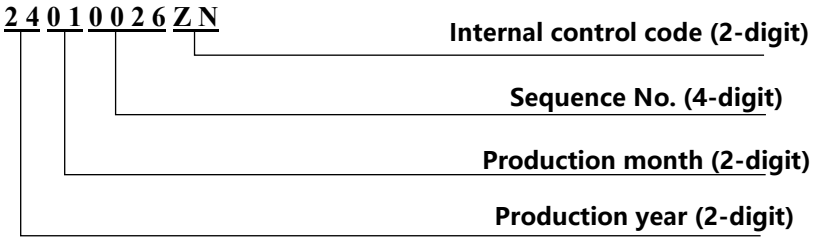
5. Definition of Labels

a) Open-Cell Serial Label

This label is pasted on the S-PWB.

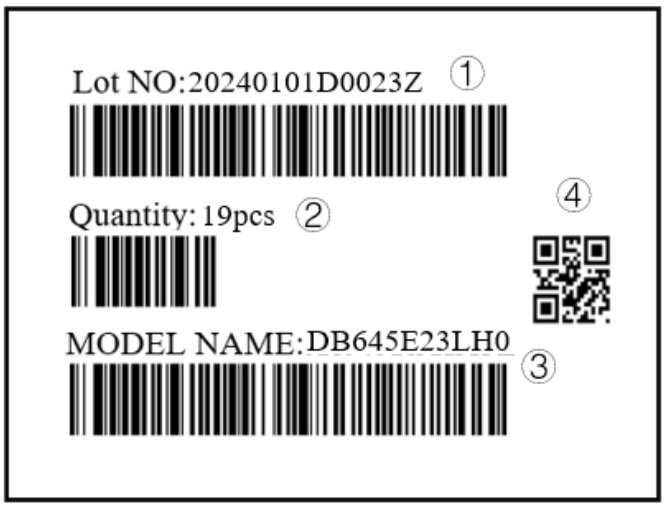
①Data Matrix: Serial No. (10-digit)
②Model No. (11-digit)
③Serial No. (10-digit) [Note1]

1) How to express Serial No.



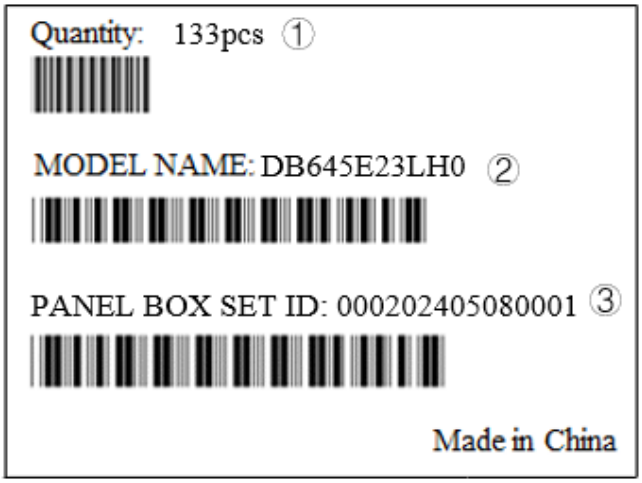
b) Open Cell Packing Label

・Label on the packing case (cell box)

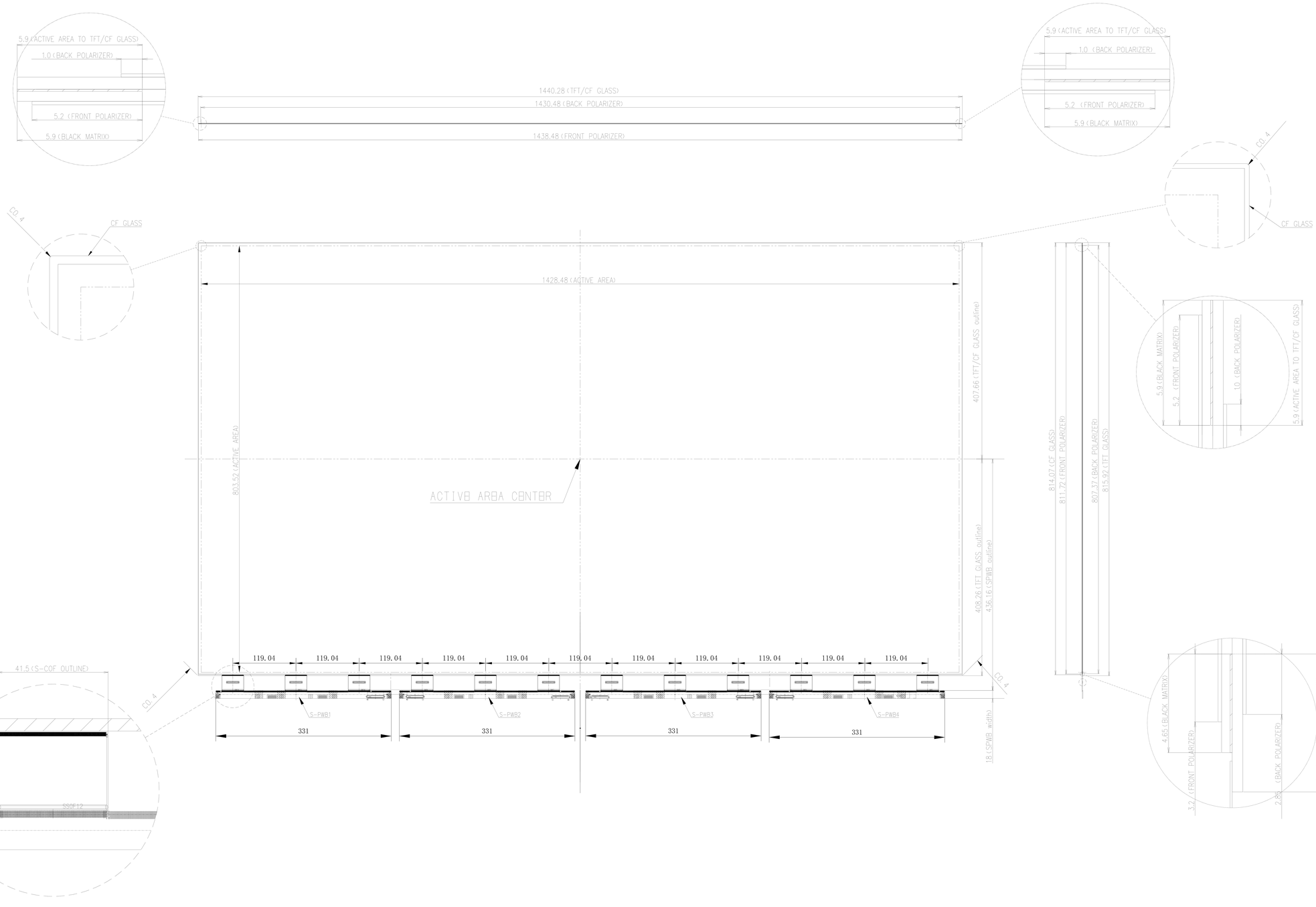


①Cell Box Lot No.(14-digit)
②Quantity
③Model No. (11-digit)
④Data Matrix: Cell Box Lot No.((14-digit)

・Label on the packing carton



①Quantity
②Model No. (11-digit)
③Panel Box Set ID (15-digit)



65inch 4K2K (GOA) 60Hz