

A close-up photograph of a television circuit board, likely an MB180V IDTV. The board is green with various electronic components. A large, dark integrated circuit (IC) is the central focus, with numerous gold-colored pins visible along its edges. To the left of the IC, there are several smaller components, including capacitors and resistors, labeled with white text: 'C108', 'C107', 'C113', 'C112', and 'U5'. The background is blurred, showing other parts of the circuit board and components.

MB180V IDTV SERVICE MANUAL

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IMPORTANT

Before removing the rear cover from the TV for servicing, make sure that no cables are fixated to the cover. Release the cables from their clamps and disconnect (if any). Failure to do so may damage the wires and/or other components of the TV.

1. INTRODUCTION

17MB180V main board is driven by Mediatek. This IC is a single chip iDTV solution that supports channel decoding, MPEG decoding, and media-center functionality enabled by a high performance AV CODEC and CPU.

This board can be driven just 50Hz UHD panels.

Key features include:

- Combo Front-End Demodulator
- A multi standart A/V format decoder
- The MACEpro video processor
- Home theatre sound processor
- Rich internet connectivity and completed digital home network solution
- Dual-stream decoder for 3D contents
- Multi-purpose CPU for OS and multimedia
- Peripheral and power management
- Embedded DRAM (for connected option)

Supported peripherals are:

- 1 RF input VHF I, VHF III, UHF
- 1 Satellite input
- 3xSide HDMI input (with ARC option from 2nd input)
- 1 Common interface(Common)
- 1 Optic/ Quax S/PDIF output
- 1 Headphone(Common)
- 2 USB(1X Side Common, 1X Side Optional(Dual-port)) and 1x internal USB for Wifi/Bluetooth
- 1 Ethernet-RJ45
- External Keypad/Tact Switch

B. PLACEMENT OF BLOCKS

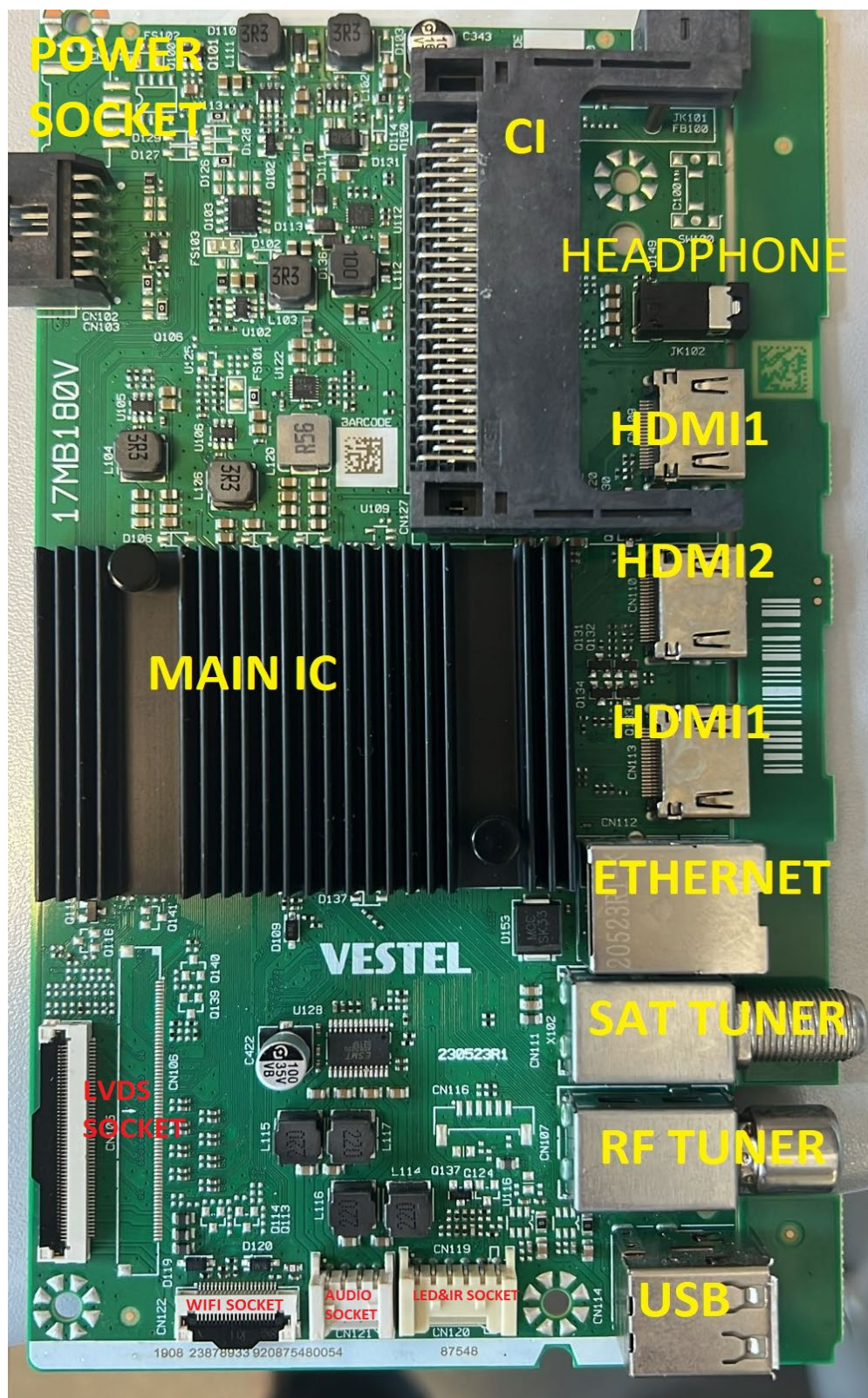


Figure 2: Board Inputs/Outputs

2. T/T2/C/A TUNER (U107)

Description:

The Si2151 is Silicon Labs' sixth-generation hybrid TV tuner supporting all worldwide terrestrial and cable TV standards. Requiring no external balun, SAW filters, wirewound inductors or LNAs, the Si2151 offers the lowest-cost BOM for a hybrid TV tuner. Also included are an integrated power-on reset circuit and an option for single power supply operation. As with prior-generation Silicon Labs TV tuners, the Si2151 maintains very high linearity and low noise to deliver superior picture quality and a higher number of received stations when compared to other silicon tuners. The Si2151 offers increased immunity to WiFi and LTE interference, eliminating the need for external filtering. For the best performance with next-generation digital TV standards, such as DVB-T2/C2, the Si2151 delivers industry-leading phase noise performance.

Features:

- Worldwide hybrid TV tuner
 - Analog TV: NTSC, PAL/SECAM
 - Digital TV: ATSC/QAM, DVBT2/T/C2/C, ISDB-T/C, DTMB
- 1.7 MHz, 6 MHz, 7 MHz, 8 MHz, and 10 MHz channel bandwidths
- 42-1002 MHz frequency range
- Industry-leading margin to A/74, NorDig, DTG, ARIB, EN55020, OpenCable™,DTMB
- Lowest BOM for a hybrid TV tuner
 - No balun, SAW filters, or external inductors required
 - Increased ESD protection on 4pins
- Best-in-class real-world reception
 - Lowest phase noise
 - High Wi-Fi and LTE immunity
- Low power consumption
 - 3.3 V and 1.8 V power supplies
 - Integrated 1.8 V LDO for 3.3 V singlesupply operation
- Integrated power-on reset circuit
- Standard CMOS process
- 3x3 mm, 24-pin QFN package
- RoHS compliant

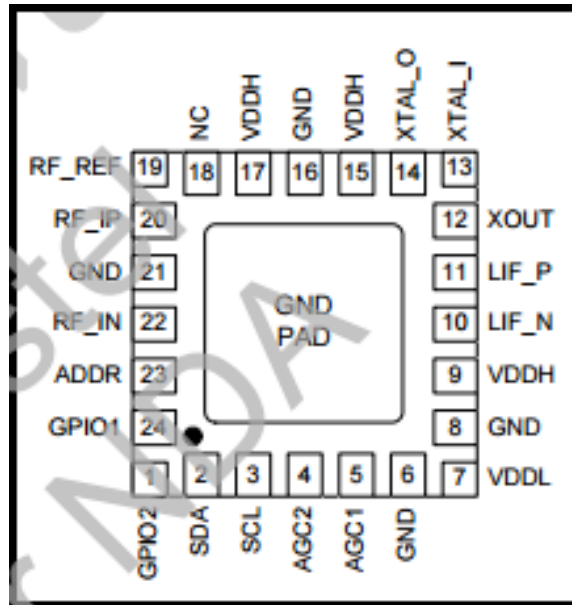


Figure 3: Si2151 Pin Description

Pin Number(s)	Name	I/O	Description
1*	GPIO2	I/O	General purpose input/output #1
2	SDA	I/O	I ² C data input/output
3	SCL	I	I ² C clock input
4*	AGC2	I	LIF output amplitude control input #2
5*	AGC1	I	LIF output amplitude control input #1
6	GND	S	Ground
7	VDDL	S	Low supply voltage, 1.8 V (leave caps connected for single supply case)
8	GND	S	Ground
9	VDDH	S	High supply voltage, 3.3 V
10	LIF_N	O	Negative LIF differential output to SoC or DTV/ATV demodulator
11*	LIF_P	O	Positive LIF differential output to SoC or DTV/ATV demodulator
12	XOUT	O	Output reference clock to secondary tuner or receiver
13	XTAL_I	I	Crystal pin 1 (or RCLK input driven by XOUT of another tuner or receiver)
14	XTAL_O	O	Crystal pin 2 (leave floating if XTAL_I is driven by XOUT of another tuner or receiver)
15	VDDH	S	High supply voltage, 3.3 V
16	GND	S	Ground

17	VDDH	S	High supply voltage, 3.3 V
18*	NC	NC	No connect
19	RF_REF	O	RF reference voltage output
20	RF_IP	I	RF input (positive)
21	GND	S	Ground
22	RF_IN	I	RF input (negative)
23	ADDR	I	I ² C address select
24*	GPIO1	I/O	General purpose input/output #1
*Note: Pin should be left floating if unused.			

Table 1: Si2151 Pin function

3. S/S2 TUNER (U127) OPTIONAL

Description

RT720 is a low-cost, direct-conversion tuner. Using for satellite signal receiving applications. It supports Digital Video Broadcast (DVB-S/S2) and further ABS-S or DVB-S2X applications.

RT720 directly converts the satellite signals from the LNB to baseband using a broadband I/Q down-converter. The operating frequency range extends from 250MHz to 2300MHz. The device includes an ultra low noise variable-gain LNA and a RF variable-gain amplifier, which is auto-controlled by integrated smart power detector and realize wide-dynamic range at the same time. The baseband low pass filters with variable cutoff frequency control support IF channel BW from 4MHz to 40MHz. The gain of baseband variable-gain amplifiers is controlled by VAGC pin to provide optimize ADC input power at demodulator.

RT720 has monolithic PLL architecture and integrated LDO; making the system achieves compact design with low BOM cost, and supplies single power pin to increase noise tolerance. RT720 is perfectly compliant with a small package, 20-pin QFN.

Features

- Worldwide satellite standards supported
 - ISDB-S
 - DVB-S/S2
 - DVB-S2X
 - ABS-S
- Support all satellite system 250MHz to 2300MHz Frequency Range 42-1002 MHz frequency range

- Fully integrated PLL with monolithic VCO
- Integrated Ultra low noise LNA: NF = 2.7dB
- High Dynamic Range Input
- Integrated Variable BW low-pass filters, support 4MHz to 40MHz
- Single voltage +3.3V supply
- Address Application
- Supported 16MHz, 24MHz and 27MHz crystal with CL=16pF, ESR $\leq$ 30ohm.(please reference application note)
- High RF Input ESD protection technique.
- 4 differential IQ out & 2 single IQ out.
- Two AGC control mode- positive & negative, controlled by SW
- RF & IF RSSI

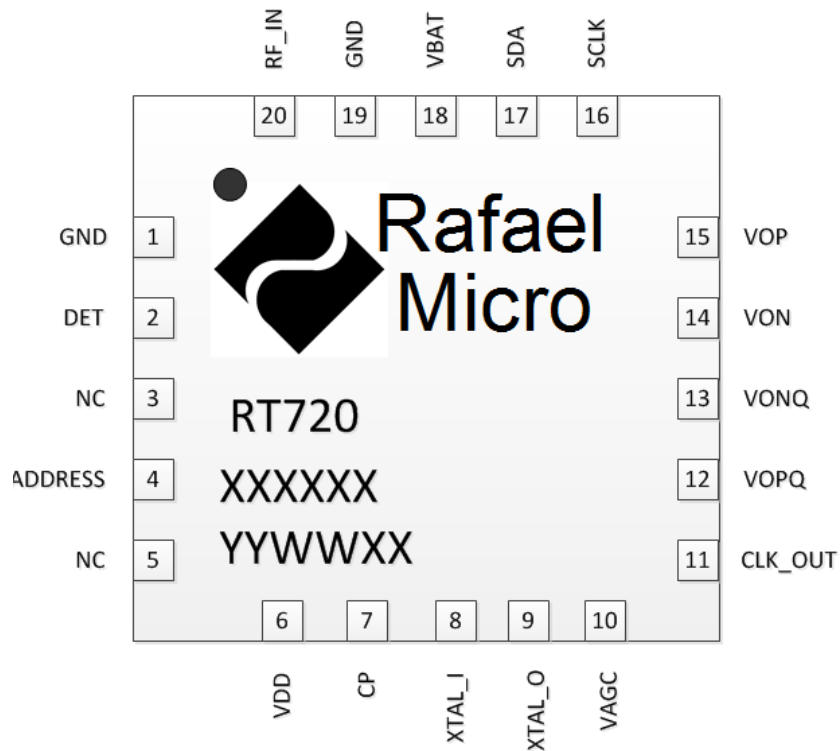


Figure 4: RT720 Pin description

Pin Number	Pin Name	I/O	Description
1	GND	S	GND
2	DET	-	RFAGC decoupling
3	NC	-	NC
4	Address	-	Address
5	NC	-	NC
6	VDD	S	3V3 LDO Input
7	CP	-	PLL Charge Pump Output (Off-chip Loop Filter needed)
8	XTAL_I	I	Crystal Input
9	XTAL_O	I	Crystal Output
10	VAGC	I	Voltage Gain Control Input
11	CLK_OUT	O	Clock Output for demodulator (Frequency = Crystal Frequency)
12	VOPQ	O	Quadrature Baseband Differential Output.
13	VONQ	O	Quadrature Baseband Differential Output.
14	VON	O	In-Phase Baseband Differential Output.
15	VOP	O	In-Phase Baseband Differential Output.
16	SCLK	I	I ² C Clock(Built-in the pull high resistance)
17	SDA	I/O	I ² C Data(Built-in the pull high resistance)
18	VBAT	S	Internal 3V decouple
19	GND	-	GND
20	RF_IN	I	RF input. (250MHz ~ 2300MHz)

Table 2: RT720 Pin function

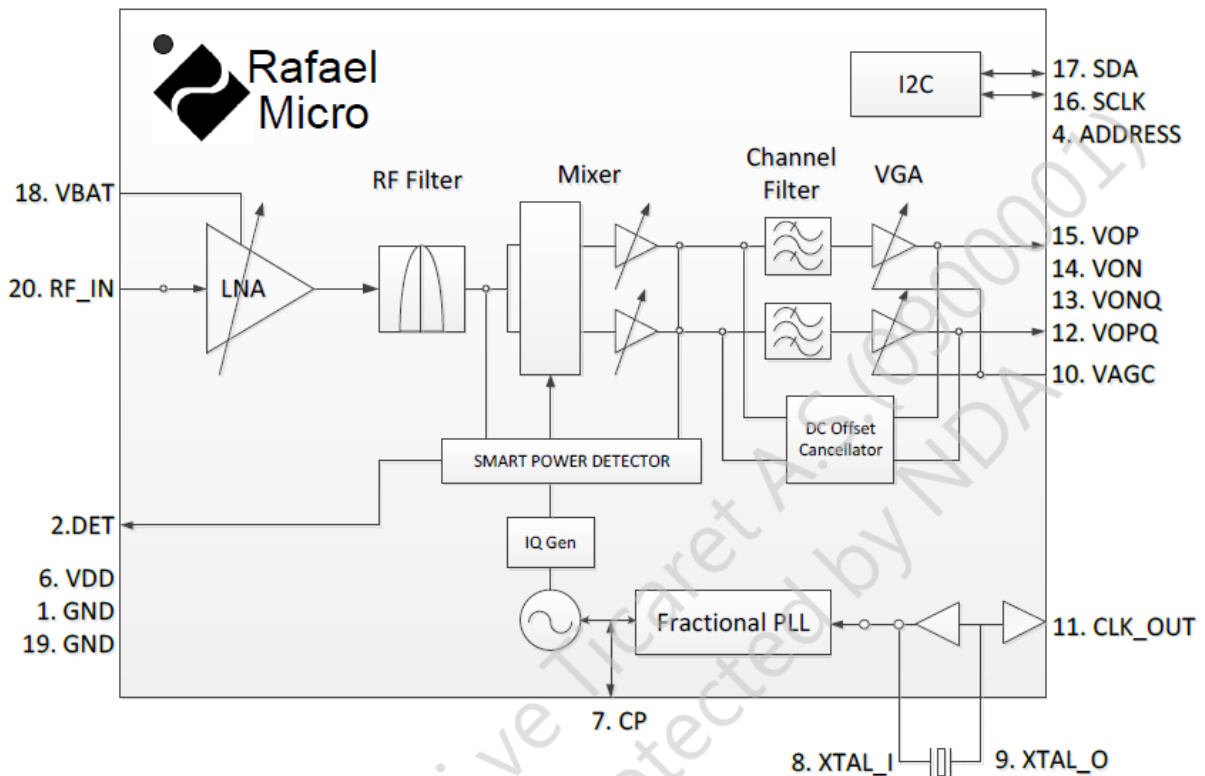


Figure 5: Block Diagram of RT720

4. AUDIO AMPLIFIER STAGES

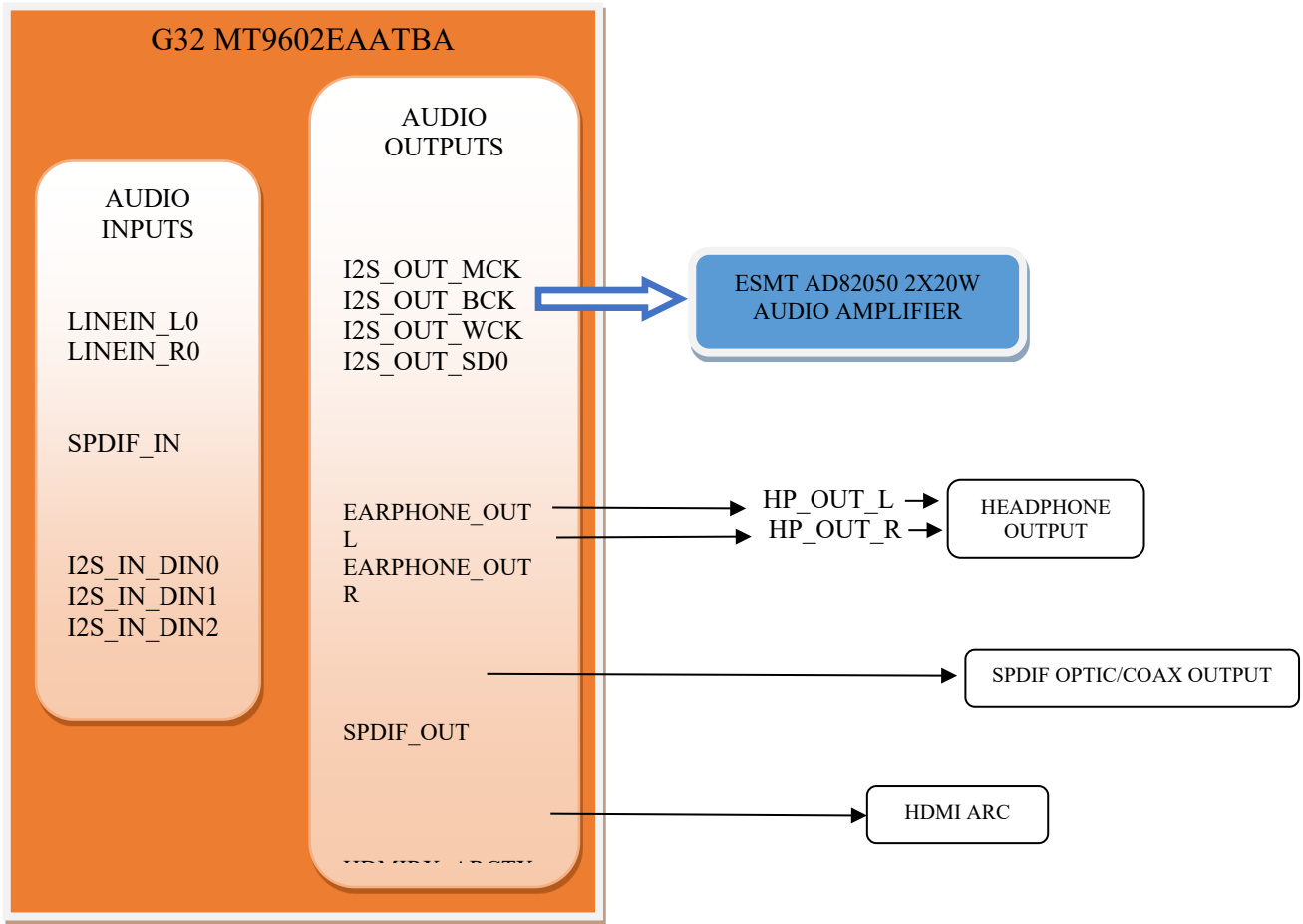


Figure 6: The block diagram of the audio part

A. MAIN AMPLIFIER (U128) (8W/10W/12W OPTIONS)

Description

AD82050 is a digital audio amplifier capable of driving 20W (BTL) each to a pair of 8Ω load speaker and 40W (PBTL) to a 4Ω load speaker operating at 24V supply without external heat-sink or fan requirement with play music.

AD82050 can provide advanced audio processing functions, such as volume control, audio mixing, and Dynamic Range Control (DRC). These are fully programmable via a simple I2C control interface. Robust protection circuits are provided to protect AD82050 from damage due to accidental erroneous operating conditions. The full digital circuit design of AD82050 is more tolerant to noise and PVT (Process, Voltage, and Temperature) variation than the analog class-AB or class-D audio amplifier counterpart implemented by analog circuit design. AD82050 is pop-free during instantaneous powered on/off or mute/shut down switching because of its robust built-in anti-pop circuit.

Features

- 16/18/20/24-bits input with I2S, Left-alignment, Right-alignment and TDM data format
- PSNR & DR (A-weighting) Loudspeaker: 104dB (PSNR), 108dB (DR) @ 24V
- Multiple sampling frequencies (Fs)
 - 8kHz / 16kHz / 32kHz and
 - 44.1kHz / 48kHz and
 - 88.2kHz/96kHz
- System clock = 32x, 48x, 64x, 96x, 128x, 192x, 256x Fs
- Supply voltage
 - 3.3V for digital circuit
 - 4.5V~26V for loudspeaker driver
- Supports 2.0CH/Mono configuration
- Loudspeaker output power for Stereo@ 12V
 - 7W x 2ch into 8Ω < 1% THD+N
 - 10W x 2ch into 8Ω < 1% THD+N
- Loudspeaker output power for Stereo@ 18V
 - 15W x 2ch into 8Ω < 1% THD+N
- Loudspeaker output power for Stereo@ 24V
 - 20W x 2ch into 8Ω < 1% THD+N
- Sounds processing including:
 - Volume control (+24dB~-103dB, 0.125dB/step)
 - Dynamic range control
 - Power clipping
 - Channel mixing
 - User programmed noise gate with hysteresis window
 - Noise gate with hysteresis window
 - Pre-scale/post-scale
 - DC-blocking high-pass filter
 - I2S output with user programmed gain (+24dB~mute)
- Anti-pop design
- I2S output with selectable Audio DSP point
- Short circuit and over-temperature protection

- Support I2C control without clock
- I2C control interface with selectable device address
- Support software reset
- Internal PLL
- LV Under-voltage shutdown and HV Under-voltage detection
- Over voltage protection
- Power saving mode
- Dynamic temperature control

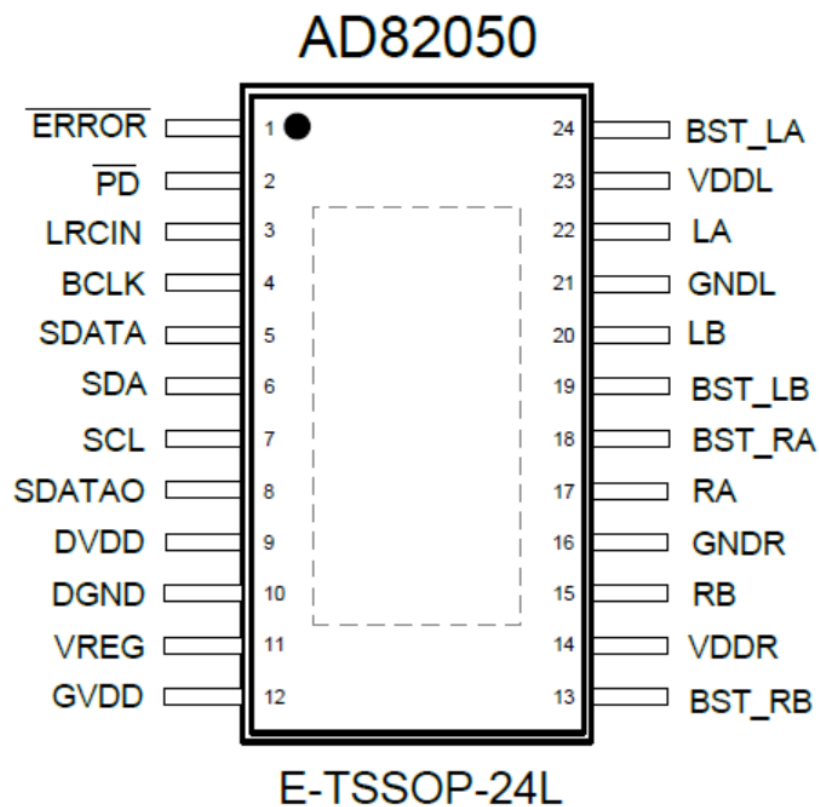


Figure 7: Pin description

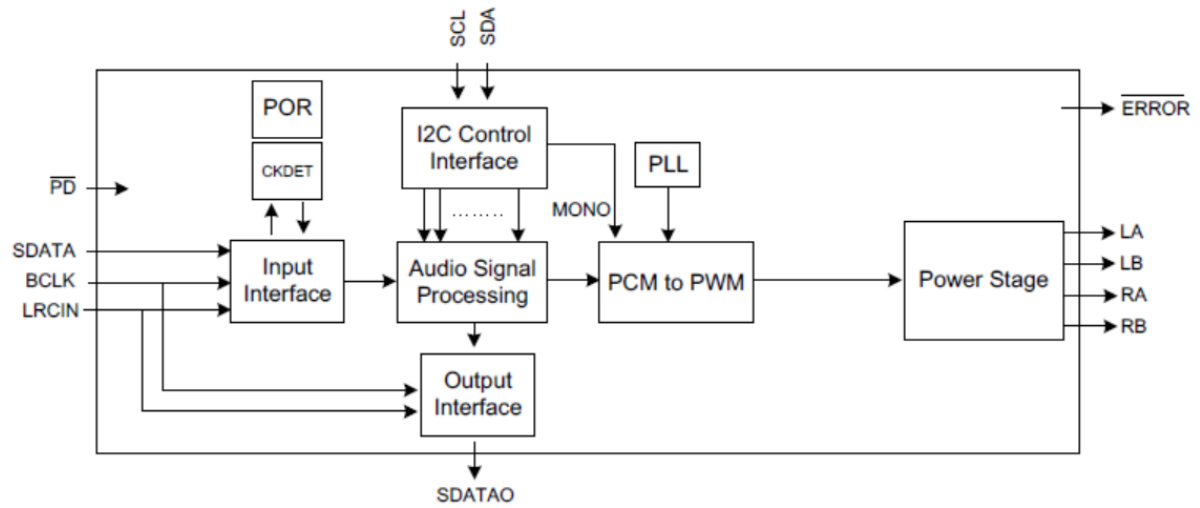


Figure 8: Functional Block Diagram

Symbol	Parameter	Min	Max	Units
DVDD	Supply for Digital Circuit	-0.3	3.6	V
VDDL / R	Supply for Driver Stage	-0.3	30	V
V_i	Input Voltage	-0.3	3.6	V
T_{stg}	Storage Temperature	-65	150	°C
T_J	Junction Operating Temperature	0	150	°C
ESD	Human Body Model		±2K	V
	Charged Device Model		±750	V

Table 3: Absolute Maximum Ratings

Symbol	Parameter	Typ	Units
DVDD	Supply for Digital Circuit	3.0 ~ 3.6	V
VDDL / R	Supply for Driver Stage	4.5 ~ 26	V
T_J	Junction Operating Temperature	-40 ~ 125	°C
T_A	Ambient Operating Temperature	-40 ~ 85	°C

Table 4: Recommended Operating Conditions

5. POWER STAGE

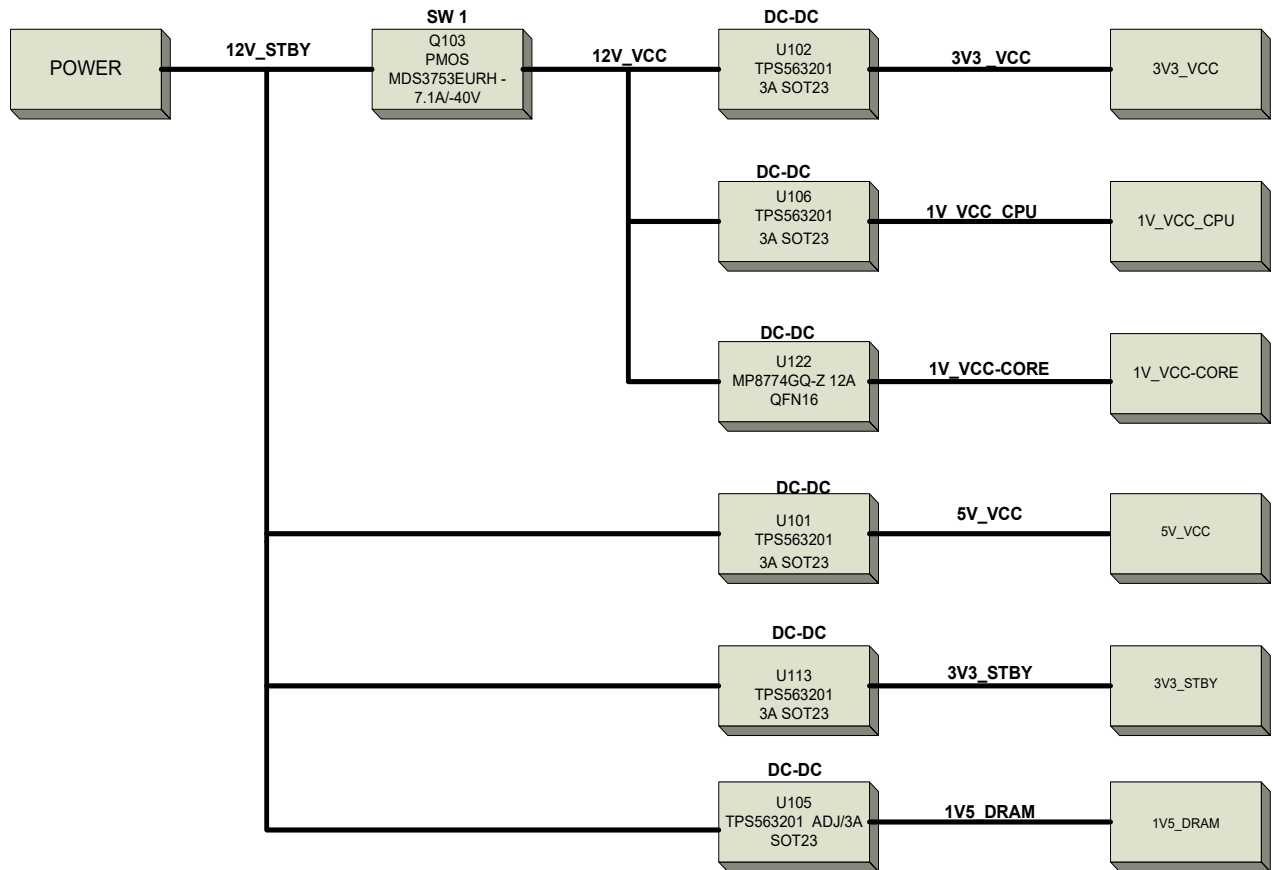


Figure 9: Power Block Diagram

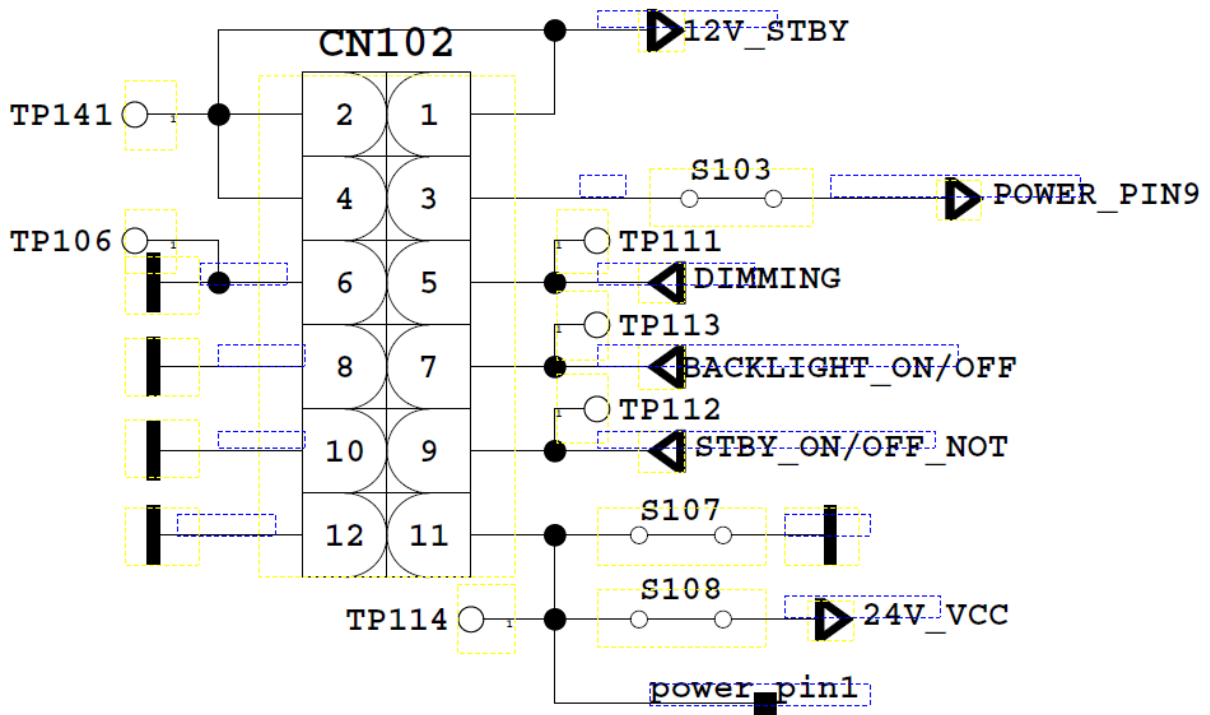


Figure 10: Power Socket and Power Options

Power socket is used for taking voltages which are 24V_VCC, 12V_STBY . These voltages are produced in power card. Also socket is used for giving dimming, backlight and standby signals with power card.

24V_VCC goes directly to the audio part. 12V_STBY is converted several different voltages on the mainboard which are shown in below figure.

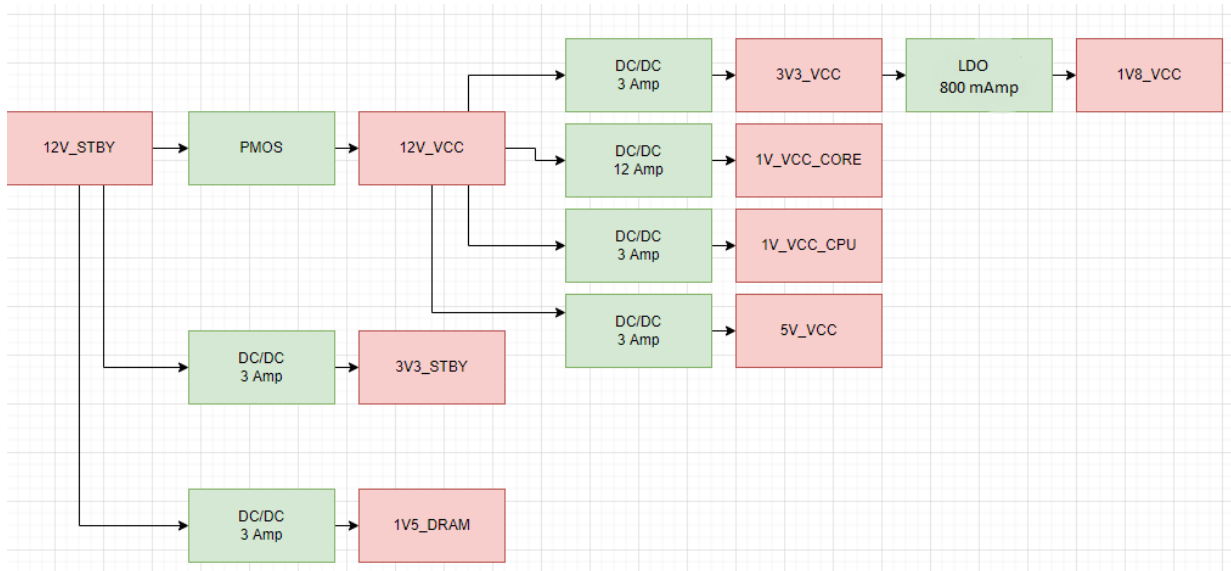


Figure 11: Power Block Diagram

List of the components:

- PMOS(Q101) → KI5P02DV
- PMOS(Q103) → MDS3753EURH
- DC-DC-1(U122) → MP8774
- DC-DC-2(U101,U102,U105,U113,U106) → TPS563201-3A
- LDO(U120) → LM1117

A. KI5P02DV (Q101)

Features

- $V_{DS} (V) = -20V$
- $I_D = -4.6 A$
- $R_{DS(ON)} < 40m\Omega$ ($V_{GS} = -4.5V$)
- $R_{DS(ON)} < 70m\Omega$ ($V_{GS} = -2.5V$)
- Low Input/Output Leakage

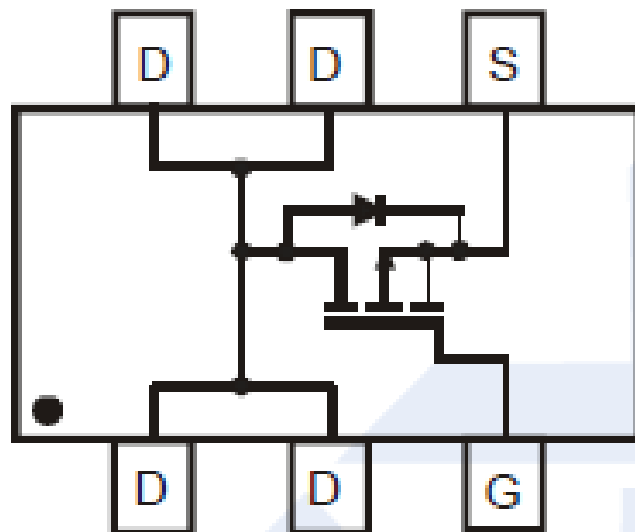


Figure 12: Pin description

■ Electrical Characteristics Ta = 25°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V _{DSS}	I _D =-250 μ A, V _{GS} =0V	-20			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-20V, V _{GS} =0V			-1	μ A
Gate-Body leakage current	I _{GSS}	V _{DS} =0V, V _{GS} = $\pm$ 12V			$\pm$ 100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250 μ A	-0.6		-1.2	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =-4.5V, I _D =-4.6A			40	m Ω
		V _{GS} =-2.5V, I _D =-3.8A			70	
On state drain current	I _{D(ON)}	V _{GS} =-4.5V, V _{DS} =-5V	-15			A
Forward Transconductance	g _{FS}	V _{DS} =-10V, I _D =-4.6A		9		S
Input Capacitance	C _{iss}	V _{GS} =0V, V _{DS} =-15V, f=1MHz		820		pF
Output Capacitance	C _{oss}			200		
Reverse Transfer Capacitance	C _{rss}			160		
Gate resistance	R _g	V _{GS} =0V, V _{DS} =0V, f=1MHz		2.5		Ω
Total Gate Charge	Q _g	V _{GS} =-4.5V, V _{DS} =-10V, I _D =-4.5A		10.1		nC
Gate Source Charge	Q _{gs}			1.5		
Gate Drain Charge	Q _{gd}			4.3		
Turn-On DelayTime	t _{d(on)}	V _{DS} = -10V, V _{GS} = -4.5V, I _D = -1A, R _G = 6 Ω		4.4		ns
Turn-On Rise Time	t _r			9.9		
Turn-Off DelayTime	t _{d(off)}			28		
Turn-Off Fall Time	t _f			23.4		
Maximum Body-Diode Continuous Current	I _S				-1.7	A
Diode Forward Voltage	V _{SD}	I _S =-2.1A, V _{GS} =0V	-0.5		-1.4	V

Figure 13: Electrical Characteristic

B. MDS3753EURH (Q103)

Features

- V_{DS} (V) =-40V
- I_D =-7.1 A
- R_{DS(ON)} < 30m Ω (V_{GS} =-10V)
- R_{DS(ON)} < 37m Ω (V_{GS} =-4.5V)
- Low Input/Output Leakage

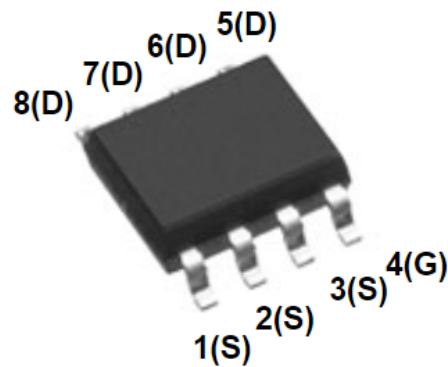


Figure 14: Pin description

Electrical Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Characteristics	Symbol	Test Condition	Min	Typ	Max	Unit
Static Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = -250\mu A, V_{GS} = 0V$	-40	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-1.0	-1.8	-3.0	
Drain Cut-Off Current	I_{DSS}	$V_{DS} = -40V, V_{GS} = 0V$	-	-	-10	μA
Gate Leakage Current	I_{GSS}	$V_{GS} = \pm 16V, V_{DS} = 0V$	-	-	± 10	
Drain-Source ON Resistance	$R_{DS(ON)}$	$V_{GS} = -10V, I_D = -3.3A$	-	20	30	m Ω
		$V_{GS} = -4.5V, I_D = -3.3A$	-	27	37	
Forward Transconductance	g_{FS}	$V_{DS} = -10V, I_D = -3.3A$		14	-	S
Dynamic Characteristics						
Total Gate Charge	Q_g	$V_{DD} = -32V, I_D = -4.7A, V_{GS} = -10V$	-	32.7	-	nC
Gate-Source Charge	Q_{gs}		-	4.1	-	
Gate-Drain Charge	Q_{gd}		-	7.4	-	
Input Capacitance	C_{iss}	$V_{DS} = -15V, V_{GS} = 0V, f = 1.0MHz$	-	1423	-	pF
Reverse Transfer Capacitance	C_{rss}		-	129	-	
Output Capacitance	C_{oss}		-	221	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = -10V, V_{DD} = -20V, I_D = -3.3A$ $R_{GEN} = 4.7\Omega$	-	14.7	-	ns
Turn-On Rise Time	t_r		-	7.1	-	
Turn-Off Delay Time	$t_{d(off)}$		-	44.2	-	
Turn-Off Fall Time	t_f		-	9.0	-	
Drain-Source Body Diode Characteristics						
Source-Drain Diode Forward Voltage	V_{SD}	$I_S = -4.7A, V_{GS} = 0V$	-	0.81	1.2	V
Reverse Recovery Time	t_{rr}	$I_S = -4.7A, di/dt = 100A/\mu s$	-	34	-	ns
Reverse Recovery Charge	Q_{rr}		-	36.5	-	nC

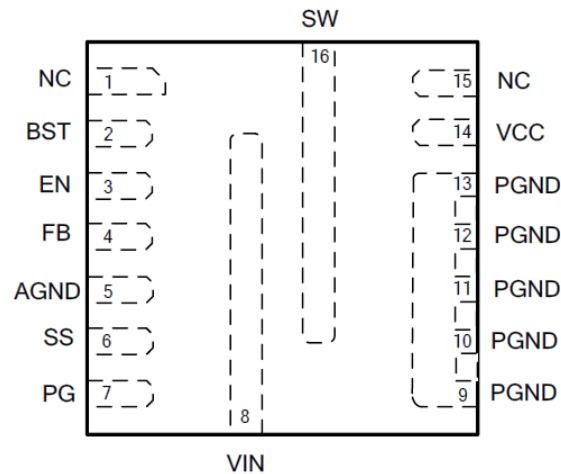
Figure 15: Electrical Characteristic

C. MP8774 (U122)

Features

- Output Adjustable from 0.6V
- Wide 3V to 18V Operating Input Range
- 12A Output Current
- $16\text{m}\Omega / 5.5\text{m}\Omega$ Low $R_{DS(ON)}$ Internal Power MOSFETs
- $100\mu\text{A}$ Quiescent Current
- High-Efficiency Synchronous Mode Operation
- Pre-Biased Start-Up
- Fixed 700kHz Switching Frequency
- External Programmable Soft Start-Up Time
- Enable (EN) and Power Good (PG) for Power Sequencing
- Over-Current Protection (OCP) and Hiccup
- Thermal Shutdown

- Available in a QFN-16 (3mmx3mm) Package



Package Pin #	Name	Description
1, 15	NC	No connection. NC must be left floating.
2	BST	Bootstrap. Connect a capacitor between SW and BST to form a floating supply across the high-side switch driver. A BST resistor less than 4.7Ω is recommended.
3	EN	Enable. Pull EN high to enable the MP8774. When floating, EN is pulled down to GND and disabled by an internal 3.3MΩ resistor.
4	FB	Feedback. FB sets the output voltage when connected to the tap of an external resistor divider between output and GND.
5	AGND	Signal ground. AGND is not connected to the system ground internally. Ensure that AGND is connected to the system ground in the PCB layout.
6	SS	Soft start. Connect a capacitor across SS and GND to set the soft-start time to avoid inrush current at start-up.
7	PG	Power good output. The output of PG is an open drain. PG changes state if UVP, OCP, OTP, or OV occurs.
8	VIN	Supply voltage. The MP8774 operates from a 3 - 18V input rail. A capacitor (C1) is needed to decouple the input rail. Use a wide PCB trace to make the connection.
9 - 13	PGND	System ground. PGND is the reference ground of the regulated output voltage. PGND requires careful consideration during the PCB layout. PGND is recommended to be connected to GND with coppers and vias.
14	VCC	Internal bias supply output. Decouple VCC with a 1μF capacitor. Place the VCC capacitor close to VCC and GND.
16	SW	Switch output. Connect SW with a wide PCB trace.

Figure 16: Pin description

$V_{IN} = 12V$, $T_J = -40^{\circ}C$ to $+125^{\circ}C$, typical value is tested at $T_J = +25^{\circ}C$, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input voltage range	V_{IN}		3		18	V
Supply Current						
Supply current (shutdown)	I_{IN}	$V_{EN} = 0V$			5	μA
Supply current (quiescent)	I_Q	$V_{EN} = 2V$, $V_{FB} = 0.65V$		100	150	μA
MOSFET						
HS switch on resistance	$HS_{RDS(ON)}$	$V_{BST-SW} = 3.3V$		16		$m\Omega$
LS switch on resistance	$LS_{RDS(ON)}$	$V_{CC} = 3.3V$		5.5		$m\Omega$
Switch leakage	SW_{LKG}	$V_{EN} = 0V$, $V_{SW} = 17V$, $T_J = 25^{\circ}C$			1	μA
Current Limit and ZCD						
Valley current limit	I_{LIMIT_VY}		12	14		A
Short hiccup duty cycle ⁽⁷⁾	D_{HICCUP}			10		%
ZCD	I_{ZCD}			200		mA
Switching Frequency and Minimum On/Off Timer						
Switching frequency	F_S		600	700	800	kHz
Minimum on time ⁽⁷⁾	$T_{ON\ MIN}$			50		ns
Minimum off time ⁽⁷⁾	$T_{OFF\ MIN}$			100		ns
Reference and Soft Start						
Feedback voltage	V_{FB}	$T_J = 25^{\circ}C$	594	600	606	mV
		$T_J = -40^{\circ}C$ to $+125^{\circ}C$	591	600	609	
Feedback current	I_{FB}	$V_{FB} = 700mV$		10	50	nA
Soft-start current	I_{SS_START}		4	6	8	μA
Enable and UVLO						
EN rising threshold	$V_{EN\ RISING}$		1.1	1.25	1.4	V
EN falling threshold	$V_{EN\ FALLING}$		0.9	1	1.1	V
EN pull-down resistor	R_{EN_PD}			1.2		$M\Omega$
VCC						
VCC under-voltage lockout threshold rising	V_{CCVth}		2.6	2.8	3	V
VCC under-voltage lockout threshold	V_{CCHYS}			350		mV
VCC regulator	V_{CC}			3.4		V
VCC load regulation	Reg_{VCC}	$I_{CC} = 5mA$		3		%

$V_{IN} = 12V$, $T_J = -40^{\circ}C$ to $+125^{\circ}C$, typical value is tested at $T_J = +25^{\circ}C$, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Good						
Power good UV rising threshold	$PGUV_{vth_Hi}$		0.85	0.9	0.95	V_{FB}
Power good UV falling threshold	$PGUV_{vth_Lo}$		0.75	0.80	0.85	V_{FB}
Power good OV rising threshold	$PGOV_{vth_Hi}$		1.15	1.2	1.25	V_{FB}
Power good OV falling threshold	$PGOV_{vth_Lo}$		1.05	1.1	1.15	V_{FB}
Power good delay	PG_{Td}	Both edge		50		μs
Power good sink current capability	V_{PG}	Sink 4mA			0.4	V
Power good leakage current	I_{PG_LEAK}	$V_{PG} = 5V$			10	μA
Thermal Protection						
Thermal shutdown ⁽⁷⁾	T_{SD}			150		$^{\circ}C$
Thermal hysteresis ⁽⁷⁾	T_{SD-HYS}			20		$^{\circ}C$

Table 5: Electrical Characteristics & Maximum ratings

D. TPS563201 (U101,U102,U105,U113,U106)

General Description

The TPS54528 is an adaptive on-time D-CAP2™ mode synchronous buck converter. The TPS54528 enables system designers to complete the suite of various end-equipment power bus regulators with a cost effective, low component count, low standby current solution. The main control loop for the TPS54528 uses the D-CAP2™ mode control that provides a fast transient response with no external compensation components. The adaptive on-time control supports seamless transition between PWM mode at higher load conditions and Eco-mode™ operation at light loads. Eco-mode™ allows the TPS54528 to maintain high efficiency during lighter load conditions. The TPS54528 also has a proprietary circuit that enables the device to adapt to both low equivalent series resistance (ESR) output capacitors, such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors. The device operates from 4.5-V to 18-V VIN input. The output voltage can be programmed between 0.76 V and 6.0 V. The device also features an adjustable soft start time. The TPS54528 is available in the 8-pin DDA package, and designed to operate from –40°C to 85°C.

Features

- TPS563201 and TPS563208 3-A Converter Integrated 95-mΩ and 57-mΩ FETs
- D-CAP2™ Mode Control with fast transient response
- Input Voltage Range: 4.5 V to 17 V
- Output Voltage Range: 0.76 V to 7 V
- Pulse-skip mode
- 580-kHz Switching Frequency
- Low Shutdown Current Less than 10 μA
- 2% Feedback Voltage Accuracy (25 °C)
- Startup from Pre-Biased Output Voltage
- Cycle-by-Cycle Overcurrent Limit
- Hiccup-mode Overcurrent Protection
- Non-Latch UVP and TSD Protections
- Fixed Soft Start: 1.0 ms

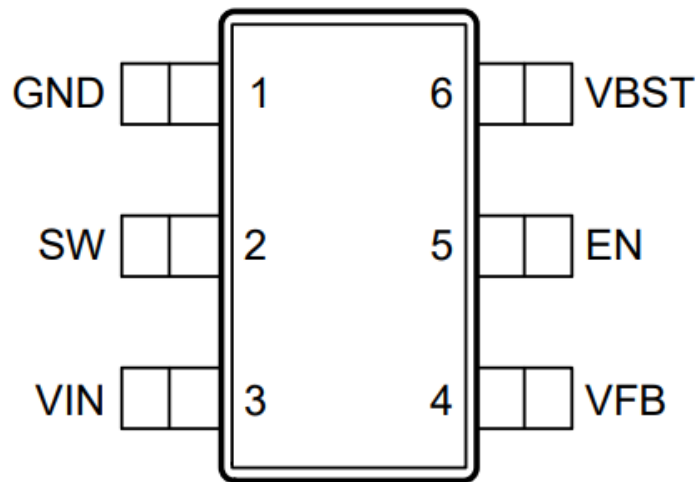


Figure 17: Pin Assignment

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	1	—	Ground pin Source terminal of low-side power NFET as well as the ground terminal for controller circuit. Connect sensitive VFB to this GND at a single point.
SW	2	O	Switch node connection between high-side NFET and low-side NFET.
VIN	3	I	Input voltage supply pin. The drain terminal of high-side power NFET.
VFB	4	I	Converter feedback input. Connect to output voltage with feedback resistor divider.
EN	5	I	Enable input control. Active high and must be pulled up to enable the device.
VBST	6	O	Supply input for the high-side NFET gate drive circuit. Connect 0.1 μ F capacitor between VBST and SW pins.

$T_J = -40^{\circ}\text{C}$ to 125°C , $V_{IN} = 12\text{ V}$ (unless otherwise noted)

40 °C to 125 °C; $V_{IN} = 12\text{ V}$ (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{VIN}	Operating – non-switching supply current	V_{IN} current, $EN = 5\text{ V}$, $V_{FB} = 0.8\text{ V}$	TPS563201	380	520	μA
			TPS563208	590	750	
I_{VINSN}	Shutdown supply current	V_{IN} current, $EN = 0\text{ V}$		1	10	μA
LOGIC THRESHOLD						
V_{ENH}	EN high-level input voltage	EN	1.6			V
V_{ENL}	EN low-level input voltage	EN			0.8	V
R_{EN}	EN pin resistance to GND	$V_{EN} = 12\text{ V}$	225	400	900	k Ω
V _{FB} VOLTAGE AND DISCHARGE RESISTANCE						
V_{FBTH}	V_{FB} threshold voltage	$V_O = 1.05\text{ V}$, $I_O = 10\text{ mA}$, Eco-mode™ operation		774		mV
	V_{FB} threshold voltage	$V_O = 1.05\text{ V}$, continuous mode operation	749	768	787	mV
I_{VFB}	V_{FB} input current	$V_{FB} = 0.8\text{ V}$		0	±0.1	μA
MOSFET						
$R_{DS(on)h}$	High-side switch resistance	$T_A = 25^{\circ}\text{C}$, $V_{BST} - SW = 5.5\text{ V}$		95		m Ω
$R_{DS(on)l}$	Low-side switch resistance	$T_A = 25^{\circ}\text{C}$		57		m Ω
CURRENT LIMIT						
I_{ocL}	Current limit	DC current, $V_{OUT} = 1.05\text{ V}$, $L_1 = 1.5\text{ }\mu\text{H}$	3.3	4.2	5.1	A
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold ⁽¹⁾	Shutdown temperature		172		$^{\circ}\text{C}$
		Hysteresis		37		
ON-TIME TIMER CONTROL						
$t_{OFF(MIN)}$	Minimum off time	$V_{FB} = 0.5\text{ V}$		220	310	ns
SOFT START						
T_{SS}	Soft-start time	Internal soft-start time		1.0		ms
FREQUENCY						
F_{SW}	Switching frequency	$V_{IN} = 12\text{ V}$, $V_O = 1.05\text{ V}$, FCCM mode		580		kHz
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V_{UVP}	Output UVP threshold	Hiccup detect ($H > L$)		65%		
T_{HICCUP_WAIT}	Hiccup on time			1.8		ms
T_{HICCUP_RE}	Hiccup time before restart			15		ms
UVLO						
UVLO	UVLO threshold	Wake up V_{IN} voltage		4.0	4.3	V
		Shutdown V_{IN} voltage	3.3	3.6		
		Hysteresis V_{IN} voltage		0.4		

Table 6: Functional Pin Description & Electrical Characteristics

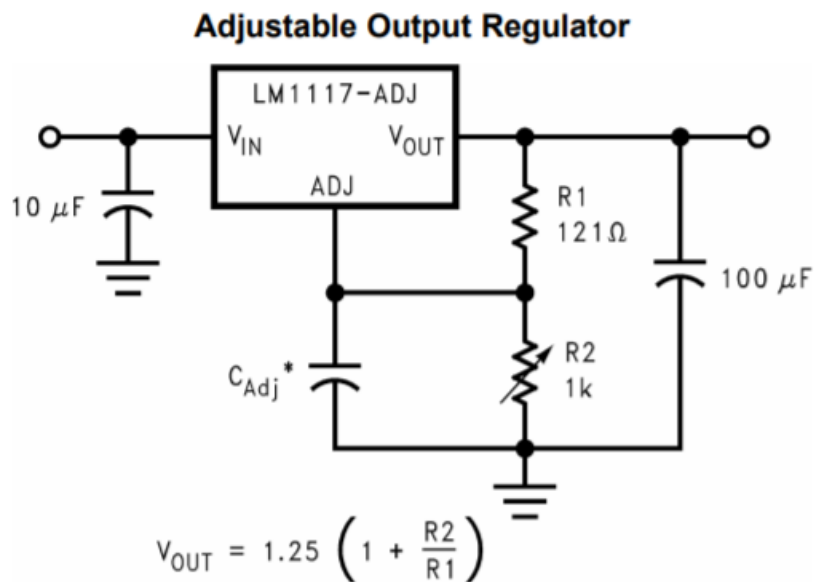
E. LM1117 (U120)

General Description

The LM1117 is a low dropout voltage regulator with a dropout of 1.2 V at 800 mA of load current. The LM1117 is available in an adjustable version which can set the output voltage from 1.25 to 13.8 V with only two external resistors. In addition, it is available in five fixed voltages, 1.8 V, 2.5 V, 3.3 V, and 5 V. The LM1117 offers current limiting and thermal shutdown. Its circuit includes a Zener trimmed bandgap reference to assure output voltage accuracy to within $\pm 1\%$. A minimum of 10- μF tantalum capacitor is required at the output to improve the transient response and stability.

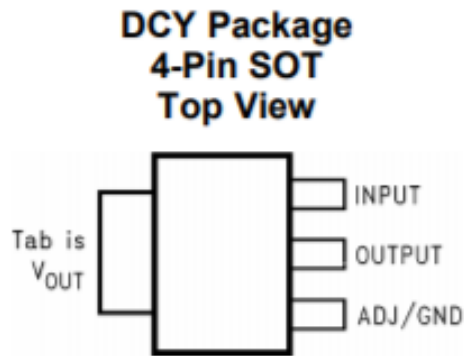
Features

- Available in 1.8 V, 2.5 V, 3.3 V, 5 V, and Adjustable Versions
- Space-Saving SOT-223 and WSON Packages
- Current Limiting and Thermal Protection
- Output Current 800 mA
- Line Regulation 0.2% (Maximum)
- Load Regulation 0.4% (Maximum)
- Temperature Range
 - LM1117: 0°C to 125°C
 - LM1117I: -40°C to 125°C



* C_{Adj} is optional, however it will improve ripple rejection.

Pin Configuration and Functions



Pin Functions

NAME	PIN					I/O	DESCRIPTION
	TO-252	WSN	SOT-223	TO-263	TO-220		
ADJ/GND	1	1	1	1	1	—	Adjust pin for adjustable output option. Ground pin for fixed output option.
V _{IN}	3	2, 3, 4	3	3	3	I	Input voltage pin for the regulator
V _{OUT}	2, TAB	5, 6, 7, TAB	2, 4	2, TAB	2, TAB	O	Output voltage pin for the regulator

Table 7: Functional Pin Description

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Maximum Input Voltage (V _{IN} to GND)			20	V
Power Dissipation ⁽²⁾		Internally Limited		
Junction Temperature (T _J) ⁽²⁾			150	°C
Lead Temperature	TO-220 (T) Package, 10 s		260	°C
	SOT-223 (MP) Package, 4 s		260	
Storage Temperature, T _{stg}		−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The maximum power dissipation is a function of T_{J(max)}, R_{θJA}, and T_A. The maximum allowable power dissipation at any ambient temperature is P_D = (T_{J(max)} − T_A)/R_{θJA}. All numbers apply for packages soldered directly into a PCB.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input Voltage (V_{IN} to GND)			15	V
Junction Temperature (T_J) ⁽¹⁾	LM1117	0	125	°C
	LM1117I	-40	125	

(1) The maximum power dissipation is a function of $T_{J(max)}$, $R_{\theta JA}$, and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly into a PCB.

6. MICROCONTROLLER

A. MEDIATEK G32 (U126)

The MT9602EAATBA is MediaTek's latest SOC solution for UHD smart TV. Based on MediaTek's advanced technologies, the MT9602EAATBA is integrated with the high-quality video processor which satisfies a variety of customer's requests for image quality to develop the state-of-the-art DTV system. The multi-core CPUs and GPUs deliver high performance for modern Linux and Android TVs. The up-to-date ARM and Mali architecture ensures the best software compatibility. Applications, such as HTML5, Java, Flash, and so on, are implemented with less efforts.

The MediaTek Professional PQ Engine includes all of MediaTek's most advanced color-tuning tools. MediaTek unique color processor with specially-designed color remapping systems assist System-developers to identify PQ characteristics of all the range of panel models quickly and easily.

The MT9602EAATBA for DTV/MM/OTT applications into a single device, reducing the overall system BOM cost. With versatile peripheral connectivity ports, like HDMI, USB, Ethernet, CVBS, etc., the MT9602EAATBA can serve as a high-quality media center in home entertainment field. To meet the increasingly popular energy legislative requirements without the use of additional hardware, the MT9602EAATBA has an ultra-low power standby mode during which an embedded MCU can act upon standby events and wake up the system as required.

1. Combo Front-End Demodulators
2. Advanced Multi-Core CPU and 3D GPU
3. 3D Formatter Engine
4. Multi-Standard A/V Format Decoder
5. MediaTek High Performance Video Processor and
MediaTek Professional PQ Engine
6. Home Theater Sound Processor
7. Internet and Variety of Connectivity Support
8. Peripheral and Power Management
9. Robust and Efficient Security Engine
10. Full Multi-Media Decoders Including AV1/ HEVC

Decoder Supporting up to FHD/60fps Resolution

High Performance Micro-processor

- ARM Advanced Multi-Core Cortex CPU
- 32KB/32KB I/D cache
- 512KB L2 cache
- Supports Neon instruction sets

3D Graphic GPU

- ARM Advanced Multi-Core Mali GPU
- Vulkan 1.1
- Supports OpenGL ES 3.2/2.0/1.1
- Supports OpenCL 2.0
- Supports DirectX 11 FL9_3
- Supports rendering size up to UHD

Transport Stream De-multiplexer

Supports two parallel and one serial TS inputs interfaces, with or without sync signal

- Supports one of TS PAD is programmable TS input/output
- Supports external demodulators
- TS data rate is 140Mbit/s for serial and 56MByte/s for parallel
- 128 general purpose PID filters and 128 section filters for all transport stream demultiplexer
- Supports additional audio/video/PCR filters

- Supports time-shift
 - Supports 3DES/DES and AES encryption/decryption

MPEG-2 Video Decoder

- ISO/IEC 11172-2 MPEG-1 video format decoding
- ISO/IEC 13818-2 MPEG-2 video MP@HL and HD level
- Supports resolution up to HDTV (1080p60,1080i, 720p) and SDTV
- Supports dual stream decoding for 3D content
- Supports for FHDp60 2x fast forwarding playback

MPEG-4 Video Decoder

- ISO/IEC 14496-2 MPEG-4 ASP video decoding up to HD level
- Supports resolutions up to HDTV (1080p@60fps)
- Supports Divx Home Theater & HD profiles
- Supports FLV version1 video format decoding
- Supports dual stream decoding for 3D content

H.264 Decoder

- ITU-T H.264, ISO/IEC 14496-10(main and high profile up to level 5.2) video decoding
- Supports resolutions up to 4096x2160@fps
- Supports bitrate up to 135Mbps
- Supports resolutions for all DVB, ATSC, HDTV,DVD and VCD
- Supports SVAFF 2ES (for Dual Decode)
- Supports MVC 3D decoding up to 1080p@60fps

VP8 Decoder

- Supports Google VP8 decoder
- Supports resolution up to 1920x1080@60fps
- Supports maximum bitrate up to 50Mbps

VP9 Decoder

- Supports Google VP9 decoder
- Supports 4:2:0 subsampling and 8bit/10bit color depth
- Supports max resolution and frame rate 4096x2160@60fps
- Supports max bitrate up to 100Mbps

AVS+ DecoderOptional

- Supports Broadcasting profile, level 6.0.1.08.60(AVS+)
- Supports Jizhun profile, level 6.0
- Supports bitrate up to 50Mbps
- Supports resolution up to 1920x1080@60fps
- Supports dual stream decoding

AVS2 DecoderOptional

- Supports AVS2 video decoding
- Supports Main-10bit profile, level 8.2.60
- Supports 8-bit/10-bit color depth
- Supports resolution up to 4096x2304@60fps
- Supports max bitrate up to 100Mbps

AV1 Video Decoder Optional

- Supports AV1 video decoding
- Supports Main profile, level 5.1
- Supports 8-bit/10-bit color depth
- Supports resolution up to 4096x2304@60fps
- Supports max bitrate up to 100Mbps

LZMA Compression

- Supports ACP interface
- Supports LZMA proprietary format
- Supports fixed 4KB
- Supports Input data rate 56MB/s
- Supports Output data rate 133MB/s
- Supports Command Queue

RealMedia DecoderOptional

- Supports RV8, RV9, RV10 decoders
- Supports file formats with RM and RMVB

- Supports maximum resolution up to 1080p@60fps
- Supports Picture Re-sampling
- Supports in-loop de-block for B-frame
- Supports dual stream decoding

HEVC (H.265) Decoder

- Supports HEVC/H.265 video decoding
- Supports Main/Main-10 profile, and Scalable Main/Scalable Main-10 profile, level 5.1, hightier
- Supports 8-bit/10-bit color depth
- Supports resolution up to 4096x2160@75fps, or 4096x2160@60fps+1920x1080@60fps for Dolby Vision
- Supports max bitrate upto 100Mbps

H.264 EncoderOptional

- Supports H.264 encoding, Main Profile, level 4.1
- Maximum output frame-rate/resolution: 1920x1080@30fps, 1280x720@60fps
- Supports MVs: 16x16, 16x8, 8x16, 8x4, 4x8, 4x4
- Supports up to quarter-pel
- Supports up to two reference frames

Hardware JPEG Decoder

- Supports upto 1920x1080@30fps, 1280x720@60fps
- Supports formats: 422/411/420/444/422T
- Supports scaling down ratios: 1/2x1/2, 1/4x1/4, 1/8x1/8
- Supports both color and grayscale pictures
- Supports sequential mode, single scan
- Supports programmable Region of Interest(ROI)
- Following the file header scan the hardware decoder fully handles the decode process

VC-1 Video Decoder**Optional**

- Supports SMPTE-421M (VC1 video) decoding up to AP@L3 (2048x1024p60)
- Supports dual stream decoding for 3D content

NTSC/PAL/SECAM Video Decoder

- Supports NTSC-M, NTSC-J, NTSC-4.43, PAL (B,D, G, H, M, N, I, Nc), and SECAM standards
- Automatic standard detection
- Motion adaptive 3D comb filter
- Supports CVBS & Y/C S-video inputs
- Supports Teletext and V-chip

Multi-Standard TV Sound Processor

- Supports BTSC/A2 demodulation
- Supports NICAM/FM/AM demodulation
- Supports MTS Mode Mono/Stereo/SAP in BTSC mode
- Supports Mono/Stereo/Dual in A2/NICAM mode
- Built-in audio sampling rate conversion (SRC)
- Audio processing for loudspeaker channel, including volume, balance, mute, tone, EQ, virtual stereo/surround and treble/bass controls
- Advanced sound processing options available, for example: Dolby1, DTS2, DBX-TV3
- Supports digital audio format : MPEG-1, MPEG-2 (Layer I/II), MP3, AAC-LC, HE-AAC, WMA, WMA9 Pro
- Supports Multi-stream programs : Dolby MS12-B **Optional**, Dolby MS12-D **Optional**, Dolby MS12-Y **Optional**, Dolby MS12-Z **Optional**, and DTS M6 **Optional**, DTS M6 multistream decoder/encoder
- Supports Audio Description
- Supports MPEG audio encoding
- Supports time-shifting PVR
 - Trademark of Dolby Laboratories

- Trademark of DTS, Inc. **Optional**
Please see Ordering Guide for details
- Trademark of DBX-TV, Inc.
- Supports programmable delay for audio/video synchronization

Audio Interface

- One L/R audio line-input
- One L/R output for main speaker or additional line-output
- Supports stereo headphone driver
- I2S digital audio output and input
- S/PDIF digital audio output and input **optional**
- Supports HDMI receiver ARC function
- Supports PDM input for 2/4 channels digital microphone

Analog RGB Compliant Input Ports

- Two analog ports support up to 1080P
- Supports PC RGB input up to SXGA@75Hz
- Supports HDTV RGB/YPbPr/YCbCr
- Supports Composite Sync and SOG Sync-on-Green
- Automatic color calibration

Analog RGB Auto-Configuration & Detection

- Auto input signal format and mode detection
- Auto-tuning function including phasing, positioning, offset and gain configuration
- Sync Detection for H/V Sync

DVI/HDCP/HDMI Compliant Input Ports

- Four HDMI/DVI input ports
- HDMI 2.0b/1.4b Compliant
- HDMI 2.1
 - Max bit rate upto 6Gbps in TMDS
 - VRR and Dynamic HDR EM packet
- MediaTek iSwitch for fast HDMI switching
- HDCP 2.2/1.4 Compliant
- Supports HDMI CEC

- Supports HDMI ARC TX
- Robust receiver with excellent long-cable support

MediaTek High Performance Video Processor

- Video Processing Engine
 - Supports up to 4K UHD@60p
 - 10/12-bit Internal Data Processing
 - Arbitrary Frame Rate Conversion
- Video Care Technology
 - Video Line Broken Artifact Detection and Removal
 - Video Detection & Repairing Technology for Lousy Inputs such as Internet Streaming
- Fully Programmable Multi-Function Scaling Engine
 - High-Quality Filters with Programmable Parameter
 - An advanced Zoom Algorithm providing Aliasing/Ringing Suppression
 - Nonlinear Video Scaling supports various modes including Panorama
 - Supports Dynamic Scaling for RM, VC-1
 - Fully Programmable Zoom Ratios for Up/Down Scaling
 - Independent Horizontal and Vertical Zoom
- Deinterlacer
 - Motion Compensated Video Deinterlacing with Motion Object Stabilizer
 - Motion Adaptive Deinterlacer
 - Edge-Oriented Deinterlacer with Edge

Smoothing and Artifact Removal

- Automatic 3:2/2:2/M:N Pull-Down

Detection and Recovery

- MediaTek Genuine 3D
 - Supports Mandatory 3D Format
- Backlight Technology
 - Supports Direct and Edge Types Local
- Dimming
 - Programmable Light Spread Profile

- Content Adaptive LCD Backlight Control
- High Dynamic Range
 - Supports SMPTE ST-2084/ST-2086
 - Supports ARIB STD-B67(Hybrid Log Gamma)/BT.2100
 - Supports 2094-40 (HDR10 plus)
 - Supports ITU-R BT.2100
 - Ultra HD Premium Ready
 - Dolby Vision
- Response Time Compensation
 - Supports Overdrive Technology

MediaTek Professional PQ Engine

- UltraClear
 - MPEG Artifact Removal
 - Advanced Adaptive Block Noise Reduction
 - Advanced Mosquito Noise Cancellation
 - UltraClear Noise Reduction
 - 3D Motion-Estimation Temporal Filtering
 - 3D Noise Reduction
 - 3D Temporal Noise Reduction for Lousy Air/Cable Input
 - S-Powers
 - Video Enhancement Processor
 - Advanced 3D Independent Multi-Band Control Sharpness Technology
 - Advanced Video Enhancement Algorithm provides Aliasing/Ringing Suppression
 - Advanced Chroma Transient Improvement
 - Supports Luma Transient Improvement
- Super Resolution
- Local Detail Enhancement
- SuperiorClear Multi-Directional Anti-Aliasing and Jagged Compensation Technology
- SuperiorClear Enhance Management
- MACE
 - MediaTek Advanced Color Engine
- MediaTek Graffito Color Manager
- Color Stain Removal Technology

- Standard Color Format and Processing
- Fully Programmable Input/Output CSC
- BT601, BT709, BT2020 (CL/NCL)
- xvYCC601, xvYCC709
- AdobeRGB, AdobeYCC601
- sRGB, sYCC601
- Fully Programmable 12-bit RGB Gamma
 - Gamut Mapping
- Nonlinear/Linear RGB Domain Gamut Mapping
- Supports 2D Gamut Mapping
- Supports 3D Gamut Mapping
- Luce
 - Contrast Enhancement
- Real-Time Content Adaptive Contrast Enhancement with Chroma Compensated
- Ultra Contrast Dimming
 - SDR to HDR

Output Interface

- Single/Dual link 8/10-bit LVDS output
- Supports panel resolution up to Full HD 1920x1080@60Hz (LVDS 2ch)
- 8 lane 8/10-bit Vby1 output (configurable width: 2/4/8 lane)
- Supports panel resolution up to Ultra HD@60Hz (Vby1 8 lane)
- Supports OSD bypass to MTK FRC 120Hz/240Hz chip Optional
- Supports TCON:miniLVDS 4ch interface, panel resolution up to Ultra HD@60Hz
- Supports TCON:EPI interface, panel resolution up to Ultra HD@60Hz
- Supports TCON:CMPI interface, panel resolution up to Ultra HD@60Hz
- Supports TCON:ISP interface, panel resolution up to Ultra HD@60Hz
- Supports TCON:CHPI interface, panel resolution up to Ultra HD@60Hz
- Supports TCON:CEDS interface, panel resolution up to Ultra HD@60Hz

- Supports TCON:CSPI interface, panel resolution up to Ultra HD@60Hz
- Supports TTL output, update to 1920x1080@60Hz
- Supports programmable timing controller
- Supports dithering options
- Spread spectrum output frequency for EMI suppression
- Supports 60Hz 3D polarized panel (line interleave)
- Supports Cinema output mode

CVBS Video Encoder

- Supports all NTSC/PAL TV Standard
- Stand-alone scaling engine (no vertical scaling up)
- Programmable Hue, Contrast, Brightness
- Supports TTX/WSS output

CVBS Video Output

- Allows CVBS output of digital content to SCART

2D Graphics Engine

- Hardware Graphics Engine for responsive interactive applications
- Supports line draw, rectangle draw/fill and text draw Supports BitBlt, Stretch BitBlt, Italic BitBlt, Mirror BitBlt and Rotate BitBlt
- Supports alpha-blending operation
- Supports source/destination color key and alpha key
- Supports dither
- Supports color format conversion and format transformation
- Raster Operation (ROP)
- Supports DFB and Porter-Duff operation

VIF Demodulator

- Compliant with NTSC M/N, PAL B, G/H, I, D/K, SECAM L/L' standards
- Supports low IF architecture
- Audio/Video internal dual-path processor
- Locking range improvement

ATSC/QAM Demodulator

- ATSC A/53 compliant 8VSB
- ITU-T J.83 Annex B, SCTE DVS-031 compliant 64/256QAM receiver
- 2010 - A74 compliant
- All digital demodulation and timing recovery loops for tracking frequency and clock offset
- Automatic co-channel and adjacent channel interference suppression
- Impulse-Noise suppression
- Integrated deinterleaver RAM for Level 1 J=1 and Level 2 J= 1,2,3,4
- Supports LIF interfaces

ISDB-T DemodulatorOptional

- Compliant with ISDB-T ARIB STD-B31
- Compliant with ISDB-Tsb ARIB STD-B29
- Supports all modes defined in ISDB-T specs
- Supports all guard ratios: 1/4, 1/8, 1/16, 1/32
- Support LIF interfaces
- Impulse-noise suppression
- Phase noise compensation
- Outside-GI performance improvement
- CNR performance improvement

DVB-C Demodulator

- Compliant with ITU J.83 Annex A/C DVB-C (EN300 429)
- Supports 1-7.2 M Baud symbol rate
- Automatic blind channel scan (constellation and symbol rate)
- Supports LIF interfaces
- IIS performance improvement

DVB-T Demodulator

- Compliant with DVB-T (ETSI EN 300 744)
- Nordig 2.2.2, D-book 7.0 compliant
- Accept low IF inputs in 6, 7, 8MHz channel bandwidths
- Supports all guard intervals (1/32 to 1/4)

- Supports all constellations (QPSK, 16-QAM,64-QAM)
- Ultra fast automatic blind UHF/VHF channel scan
- Optimized for SFN channels with pre/postcursive echoes inside/outside the guard
- Phase-Noise suppression
- Impulse-Noise suppression
- All digital demodulation and timing recovery loops for tracking frequency and clock offset
- Automatic co-channel and adjacent channel interference suppression
- CNR performance improvement
- Outside-GI performance improvement

DVB-T2 DemodulatorOptional

- Compliant with DVB-T2 (ETSI EN 302 755) v1.3.1, T2-base & T2-Lite profile
- Nordig Unified 2.2.2, D-Book 7.0 compliant
- Supports all guard intervals (1/128 to 1/4)
- Supports all FFT modes from 1K to 32K
- Supports all long and short block code rates(1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 2/5, 1/3)
- Supports all constellations (QPSK, 16-QAM,64-QAM, 256-QAM)
- Transmit diversity (MISO) support
- Supports all scattered pilot patterns (PP1 toPP8)
- Supports rotated and non-rotated constellations
- Supports single and multiple PLPs
- Accept low IF inputs in 1.7, 5, 6, 7, 8MHz channel bandwidths
- All digital demodulation and timing recovery loops for tracking frequency and clock offset.
- Automatic co-channel and adjacent channel interference suppression
- Impulse-Noise suppression
- Outside GI improvement
- Locking the improvement

DVB-S DemodulatorOptional

- Compliant with DVB-S (ETSI EN 300 421)
- Data Rate: 1-70 Msps
- Code Rates: 1/2, 2/3, 3/4, 5/6, 7/8
- Carrier frequency acquisition range: 5MHz
- Fast automatic blind scan of symbol rates and carrier frequencies
- Equalizer compensates for channel impairment
- DiSEqCTM 2.0 compatible with LNB controller
- Automatic co-channel and adjacent channel interference suppression
- Impulse-Noise suppression
- All digital demodulation and timing recovery loops for tracking frequency and clock offset
- Novel carrier recovery algorithms for tracking and compensating large phase noises
- Supports Automatic FEC and Modulation
- Integrated FEC decoders for near Shannon limit performances
- Integrated signal quality and BER monitors
- Improved CNR performance

DVB-S2 DemodulatorOptional

- Compliant with DVB-S2 (ETSI EN 302 307)
- Data Rate: 1-70 Msps for QPSK , 8PSK, 16APSK, 1-57 Msps for 32APSK
- Constellations: QPSK , 8PSK , 16APSK and 32APSK
 - QPSK Code Rates: 1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 8/9, 9/10
 - 8PSK Code Rates: 3/5, 2/3, 3/4, 5/6, 8/9, 9/10
 - 16APSK Code Rates: 2/3, 3/4, 4/5, 5/6, 8/9, 9/10
 - 32APSK Code Rates: 3/4, 4/5, 5/6, 8/9, 9/10
- Supports CCM and VCM
- Supports Single Transport Stream and Multiple Transport Streams

- Roll-off factors for pulse shaping: 0.2, 0.25, and 0.35
- Carrier frequency acquisition range: 5MHz
- Fast automatic blind scan of symbol rates and carrier frequencies
- Equalizer compensates for channel impairment
- DiSEqCTM 2.0 compatible with LNB controller
- Automatic co-channel and adjacent channel interference suppression
- Impulse-Noise suppression
- All digital demodulation and timing recovery loops for tracking frequency and clock offset
- Novel carrier recovery algorithms for tracking and compensating large phase noises
- Supports Automatic FEC and Modulation
- Integrated FEC decoders for near Shannon limit performances
- Integrated signal quality and BER monitors

DVB-S2X DemodulatorOptional

- Compliant with DVB-S2 Extensions (ETSI EN302 307-2, Broadcast services except for Channel Bonding)
 - Data Rate: 1-70 Msps for QPSK , 8PSK, 8APSK-L, 16APSK, 16APSK-L, 1-57 Msps for 32APSK, and 32APSK-L
 - Constellations: QPSK , 8PSK, 8APSK-L, 16APSK, 16APSK-L, 32APSK, and 32APSK-L
 - QPSK Code Rates: 1/4, 1/3, 2/5, 1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 8/9, 9/10, 13/45, 9/20, 11/20
 - 8PSK Code Rates: 3/5, 2/3, 3/4, 5/6, 8/9, 9/10, 23/36, 25/36, 13/18
 - 8APSK-L Code Rates: 5/9, 26/45
 - 16APSK Code Rates: 2/3, 3/4, 4/5, 5/6, 8/9, 9/10, 26/45, 3/5, 28/45, 23/36, 25/36, 13/18, 7/9, 77/90
 - 16APSK-L Code Rates: 5/9, 8/15, 1/2, 3/5, 2/3

- 32APSK Code Rates: 3/4, 4/5, 5/6, 8/9, 9/10, 32/45, 11/15, 7/9
- 32APSK-L Code Rates: 2/3
- Supports CCM and VCM
- Supports Single Transport Stream and Multiple Transport Streams
- Roll-off factors for pulse shaping: 0.05, 0.1, 0.15, 0.2, 0.25, and 0.35
- Carrier frequency acquisition range: 5MHz
- Fast automatic blind scan of symbol rates and carrier frequencies
- Equalizer compensates for channel impairment
- DiSEqCTM 2.0 compatible with LNB controller
- Automatic co-channel and adjacent channel interference suppression
- Impulse-Noise suppression
- All digital demodulation and timing recovery loops for tracking frequency and clock offset
- Novel carrier recovery algorithms for tracking and compensating large phase noises
- Supports Automatic FEC and Modulation
- Integrated FEC decoders for near Shannon limit performances
- Integrated signal quality and BER monitors

Connectivity

- Three USB 2.0 host ports
- USB architecture designed for efficient support of external storage devices in conjunction with off air broadcasting
- Embedded 10/100 Ethernet PHY
- Supports Ethernet Wake-On-Lan

Miscellaneous

- DRAM interface support DDR3/4
- Supports PVR
- Parallel interface for external parallel eMMC flash and NAND flash support
- Power control module with ultra low power MCU available in standby mode

Recommended Operating Condition

Parameter	Symbol	Min	Typ	Max	Unit
3.3V Supply Voltages	V _{VDD_33}	3.14	3.3	3.46	V
1.5V Supply Voltages (DDR3)	V _{VDD_15}	1.43	1.5	1.57	V
Core Supply Voltages	V _{VDD_core}	0.921	0.95 (VID case0)	0.978	V
		0.97	1.00 (VID case1)	1.03	V
CPU Supply Voltages	V _{VDD_cpu}	0.921	0.95 (VID case0)	0.978	V
		0.97	1.00 (VID case1)	1.03	V
Ambient Operating Temperature	T _A	0		70	°C
Junction Temperature	T _J			125	°C

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
3.3V Supply Voltages	V _{VDD_33}		3.63	V
1.5V Supply Voltages	V _{VDD_15}		1.65	V
Core Supply Voltages	V _{VDD_core}		1.05	V
CPU Supply Voltages	V _{VDD_cpu}		1.26	V
Input Voltage (5V tolerant inputs)	V _{IN5Vtol}		5.3	V
Input Voltage (non 5V tolerant inputs)	V _{IN}		V _{VDD_33}	V
Storage Temperature	T _{STG}	-40	150	°C

7. GB EMMC

A. SAMSUNG EMMC 4GB KLM4G1FETE-B041 (U103)

Description

SAMSUNG eMMC is an embedded MMC solution designed in a BGA package form. eMMC operation is identical to a MMC device and therefore is a simple read and write to memory using MMC protocol v5.1 which is a industry standard. eMMC consists of NAND flash and a MMC controller. 3V supply voltage is required for the NAND area (VDDF or VCC) whereas 1.8V or 3V dual supply voltage (VDD or VCCQ) is supported for the MMC controller. SAMSUNG eMMC supports HS400 in order to improve sequential bandwidth, especially sequential read performance. There are several advantages of using eMMC. It is easy to use as the MMC interface allows easy integration with any microprocessor with MMC host. Any revision or amendment of NAND is invisible to the host as the embedded MMC controller insulates NAND technology from the host. This leads to faster product development as well as faster times to market. The embedded flash management software or FTL(Flash Transition Layer) of eMMC manages Wear Leveling, Bad Block Management and ECC. The FTL supports all features of the Samsung NAND flash and achieves optimal performance

Key Features

- Embedded MultiMediaCard Ver. 5.1 compatible.
- SAMSUNG eMMC supports features of eMMC5.1 which are defined in JEDEC Standard
 - Major Supported Features : HS400, Field Firmware Update, Cache, Command Queuing, Enhanced Strobe Mode, Secure Write Protection, Partition types
 - Non-supported Features : Large Sector Size (4KB)
- Backward compatibility with previous MultiMediaCard system specification (1bit data bus, multi-eMMC systems)
- Data bus width : 1bit (Default), 4bit and 8bit
- MMC I/F Clock Frequency : 0 ~ 200MHz

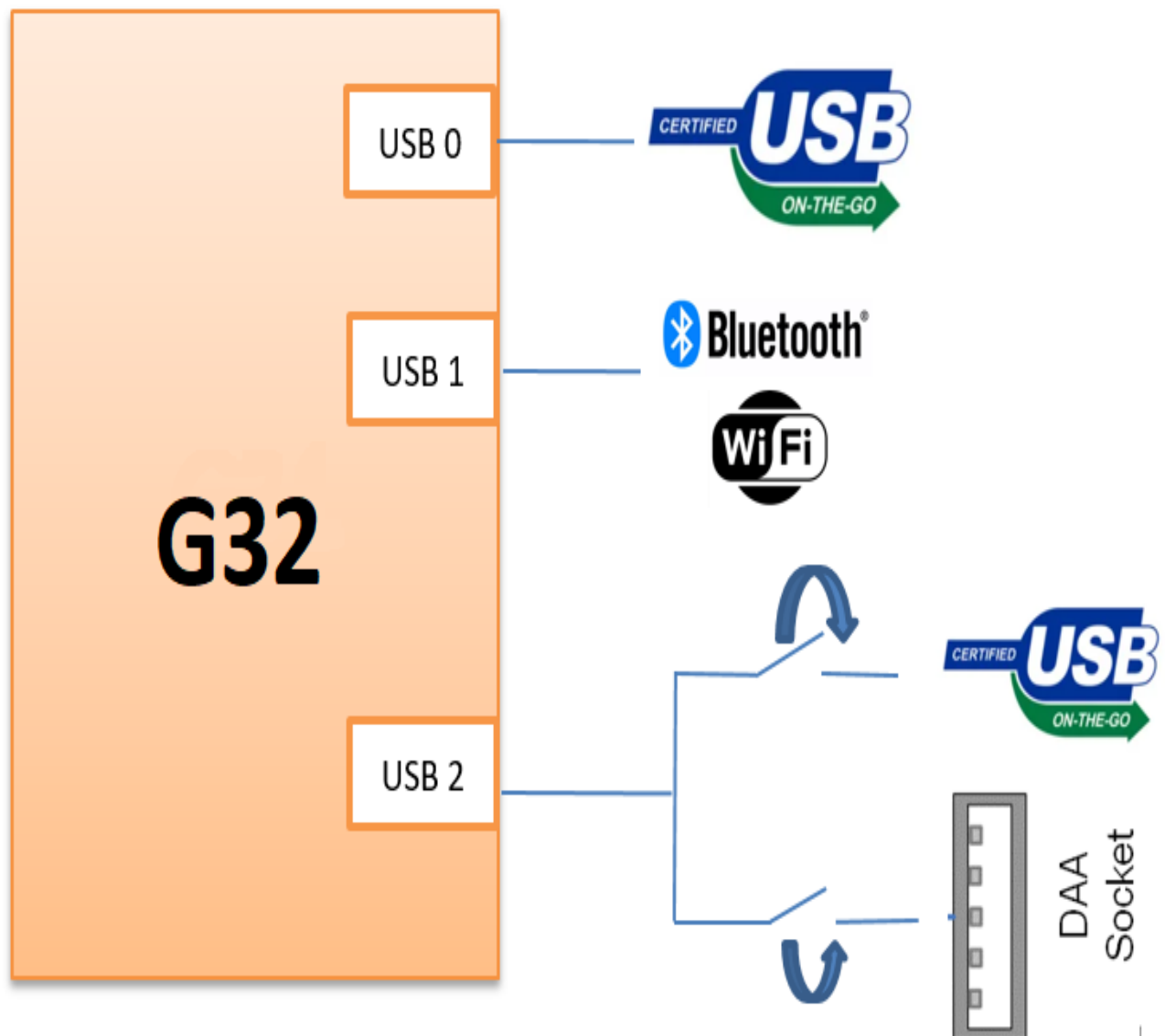
MMC I/F Boot Frequency : 0 ~ 52MHz

- Temperature : Operation (-25°C ~ 85°C), Storage without operation (-40°C ~ 85°C)
- Power : Interface power → VCCQ(1.70V ~ 1.95V), Memory power → VCC(2.7V ~ 3.6V)

Item	Min	Max	Unit
V _{CCQ}	1.70 (2.7)	1.95 (3.6)	V
V _{CC}	2.7	3.6	V
V _{SS}	-0.5	0.5	V

Table 8: Supply Voltage

8. USB INTERFACE



A. USB POWER SWITCH TPS2553-1 (U115-U116)

FEATURES

- Up to 1.5 A Maximum Load Current
- $\pm 6\%$ Current-Limit Accuracy at 1.7 A (typ)
- Meets USB Current-Limiting Requirements
- Backwards Compatible with TPS2550/51
- Adjustable Current Limit, 75 mA–1300 mA (typ)
- Constant-Current (TPS2552/53) and Latch-off (TPS2552-1/53-1) Versions
- Fast Overcurrent Response - 2- μ s (typ)
- 85-m Ω High-Side MOSFET (DBV Package)
- Reverse Input-Output Voltage Protection
- Operating Range: 2.5 V to 6.5 V
- Built-in Soft-Start
- 15 kV ESD Protection per IEC 61000-4-2 (with External Capacitance)
- UL Listed – File No. E169910 and NEMKO IEC60950-1-am1 ed2.0

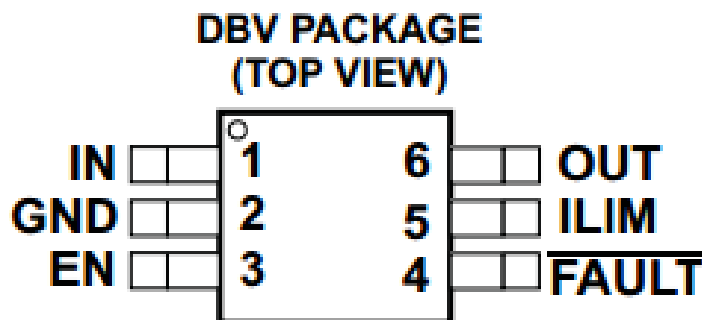
APPLICATIONS

- USB Ports/Hubs
- Digital TV
- Set-Top Boxes
- VOIP Phones

DESCRIPTION

The TPS2552/53 and TPS2552-1/53-1 power-distribution switches are intended for applications where precision current limiting is required or heavy capacitive loads and short circuits are encountered and provide up to 1.5 A of continuous load current. These devices offer a programmable current-limit threshold between 75 mA and 1.7 A (typ) via an external resistor. Current-limit accuracy as tight as $\pm 6\%$ can be achieved at the higher current-limit settings. The power-switch rise and fall times are controlled to minimize current surges during turn on/off.

TPS2552/53 devices limit the output current to a safe level by using a constant-current mode when the output load exceeds the current-limit threshold. TPS2552-1/53-1 devices provide circuit breaker functionality by latching off the power switch during overcurrent or reverse-voltage situations. An internal reverse-voltage comparator disables the power-switch when the output voltage is driven higher than the input to protect devices on the input side of the switch. The $\overline{\text{FAULT}}$ output asserts low during overcurrent and reverse-voltage conditions.



EN = Active High for the TPS2553

9. CI INTERFACE

17MB180V Digital CI Interface Block diagram:

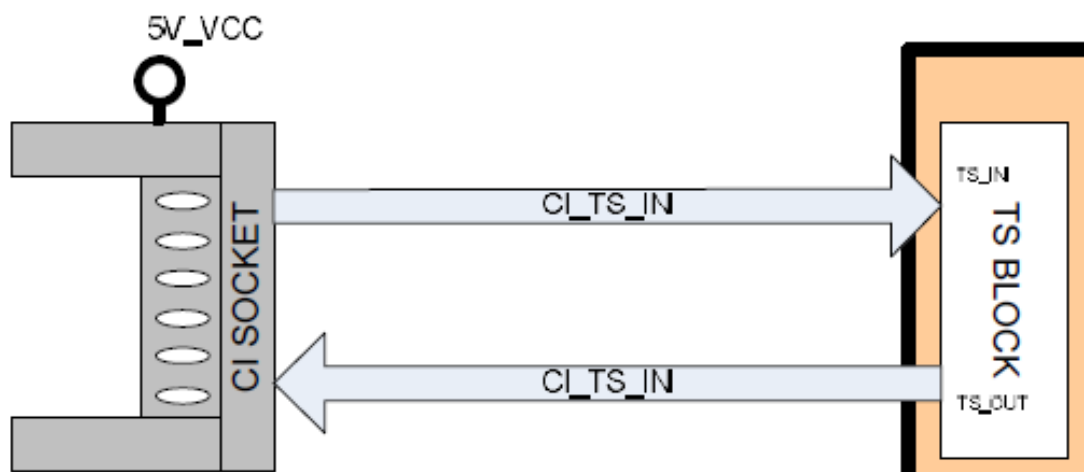


Figure 18: CI interface

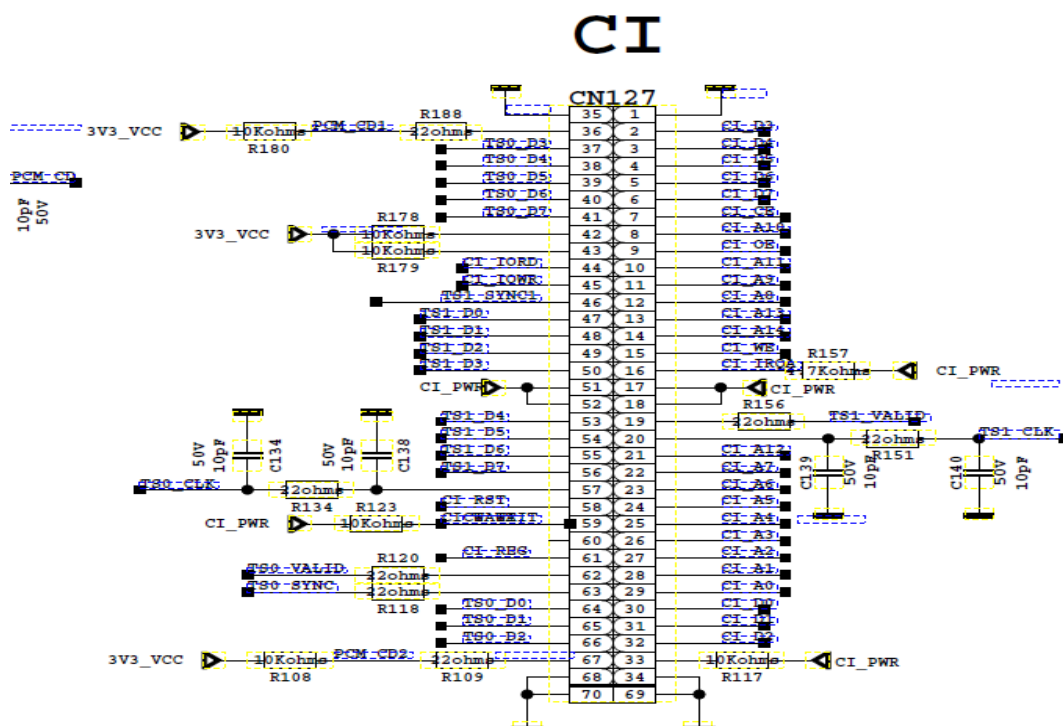


Figure 19: CI Schematic

10. SOFTWARE UPDATE

A. MAIN SOFTWARE UPDATE

In MB180V project, please follow software update procedure:

For G32(Virgo):

1. usb_MTK_DEV_EU_AIP_VGO_4K.bin document should be copied directly inside root of a flash memory (not in a folder).
2. Insert flash memory to the TV when TV is powered off.
3. While pushing the standby off/on button on remote control, then power on and wait. TV will power-up itself.
4. If First Time Installation screen comes, it means software update procedure is successful.

11. TROUBLESHOOTING

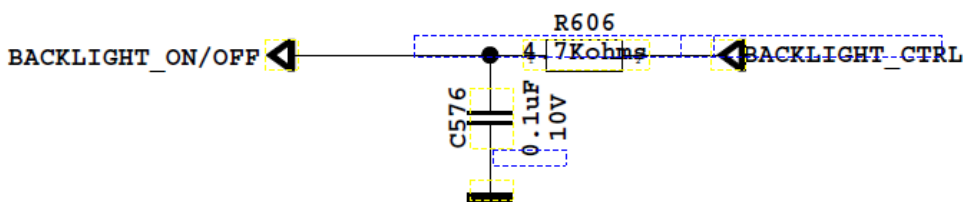
A. NO BACKLIGHT PROBLEM

Problem: If TV is working, led is normal and there is no picture and backlight on the panel.

Possible causes: Backlight pin, dimming pin, backlight supply, stby on/off pin

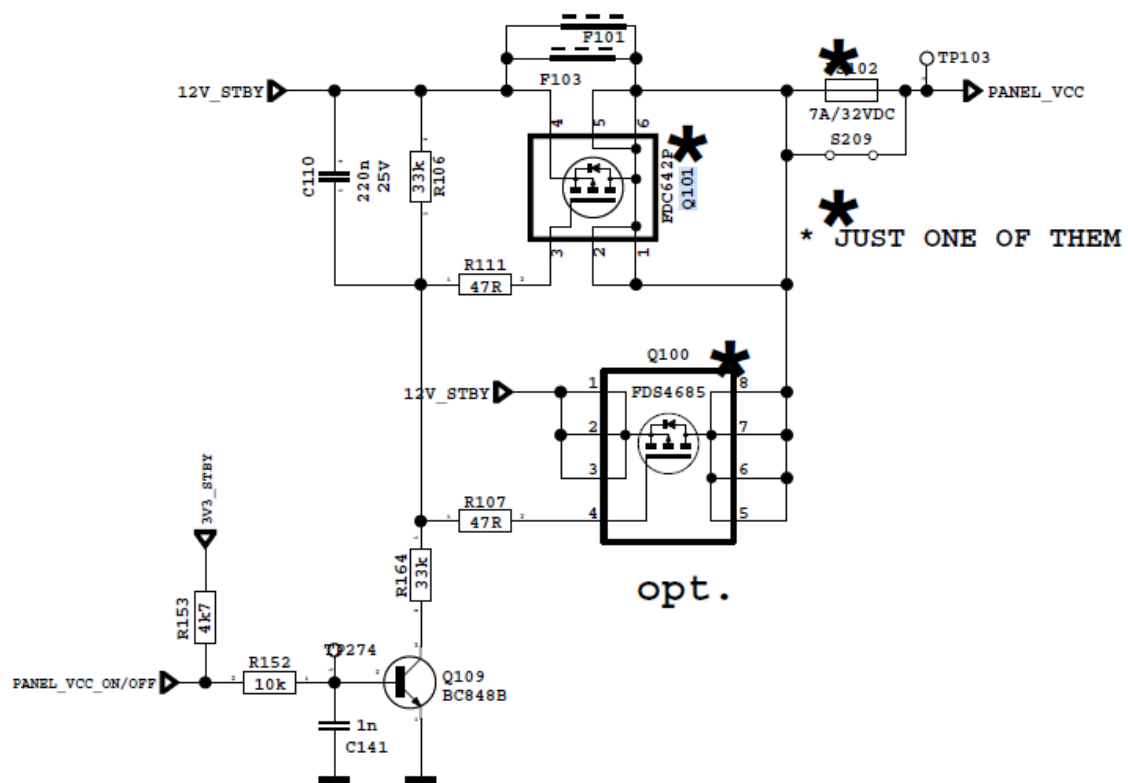
BACKLIGHT_ON/OFF pin should be high when the backlight is ON.

Backlight On/Off Circuit



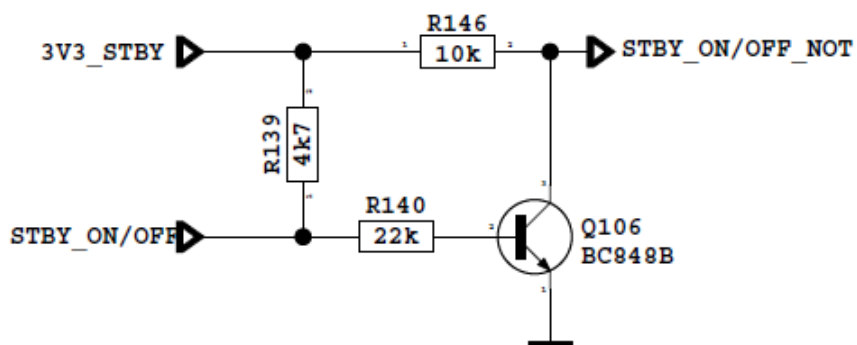
Dimming pin should be high or square wave in open position. It also can be checked at TP111. Please also check panel or power cables and connectors.

Backlight power supply should be in panel specs. Please check Q101, shown below; also it can be checked TP103.



STBY_ON/OFF_NOT should be low for TV on condition, please check Q106's collector.

STBY On/Off Circuit

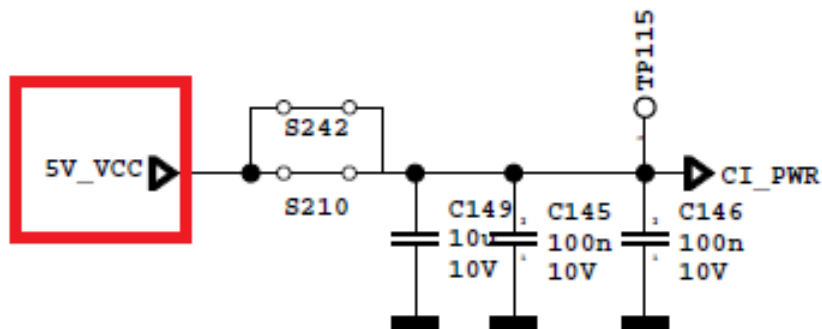


B. CI MODULE PROBLEM

Problem: CI is not working when CI module inserted.

Possible causes: Supply, supply control pin, detects pins, mechanical positions of pins.

- CI supply should be 5V when CI module inserted. If it is not 5V please check CI_PWR_CTRL, this pin should be low.



- Please check mechanical position of CI module. Is it inserted properly or not?
- Detect ports should be low. If it is not low please check CI connector pins, CI module pins.

CN127

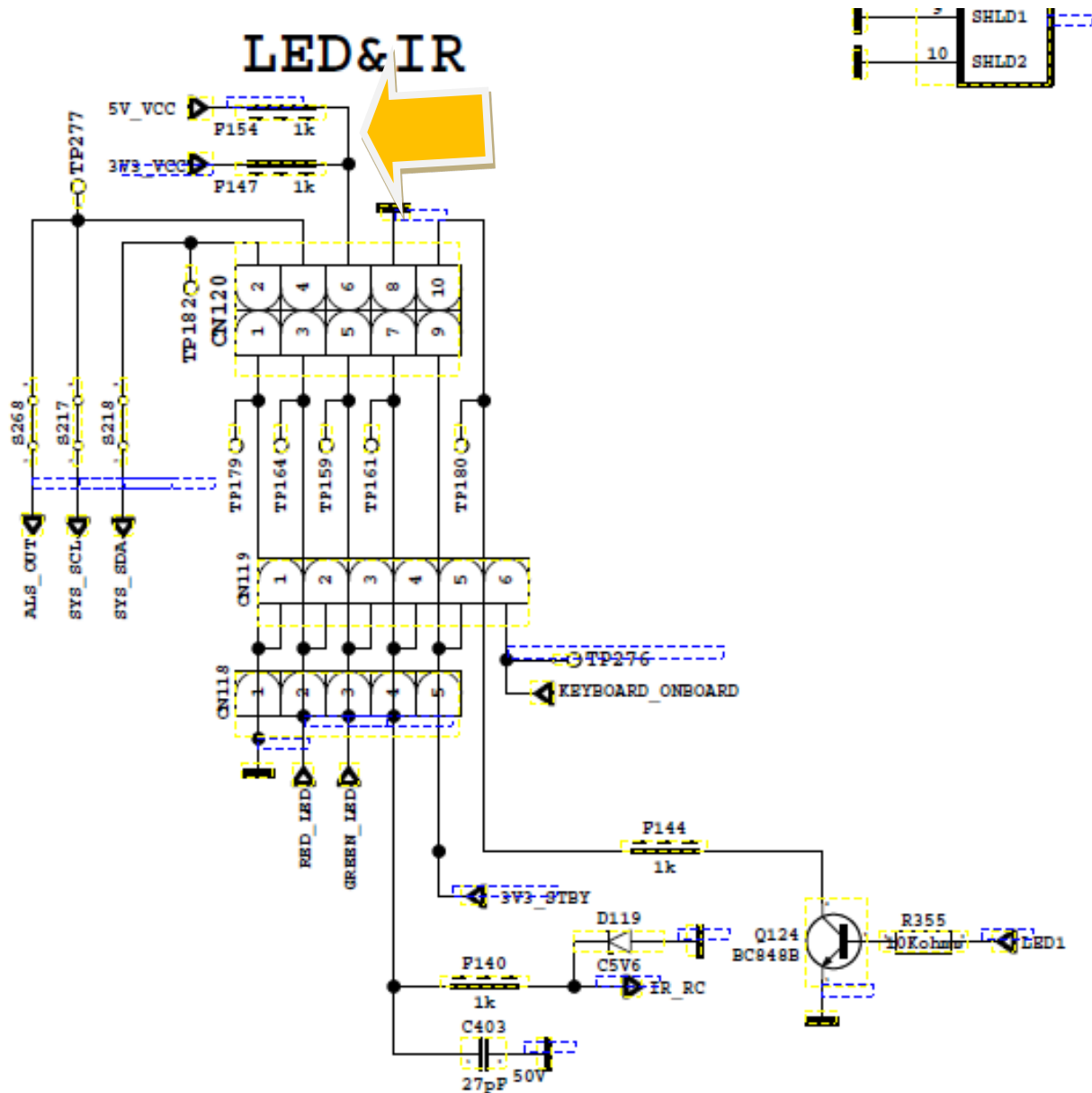


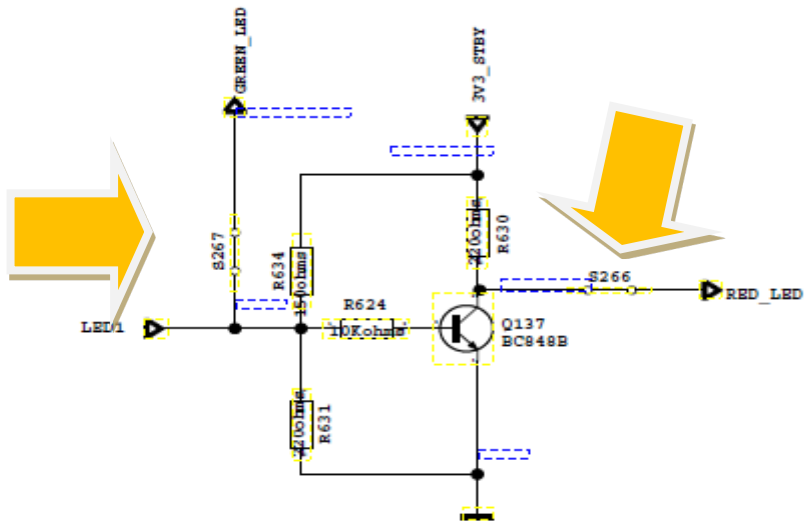
C. IR PROBLEM

Problem: LED or IR not working

Check LED card supply on MB180V chassis.

Check S266 and S267.





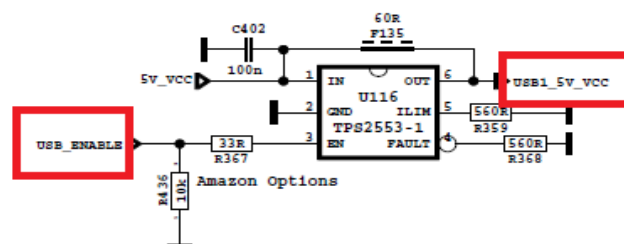
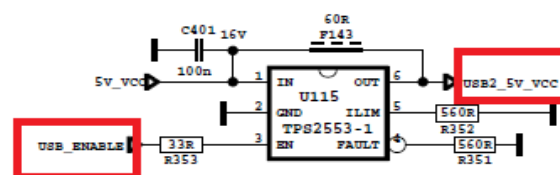
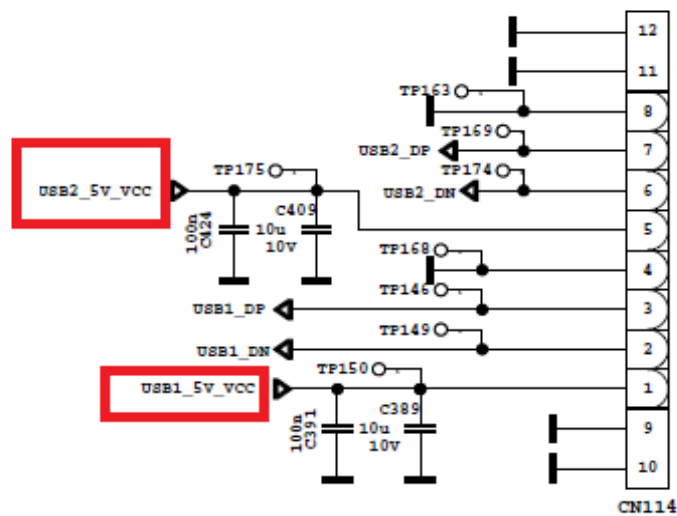
D. USB PROBLEMS

Problem: USB is not working or no USB Detection.

Check USB Supply, It should be nearly 5V. Also USB Enable should be logic high.

USB Control is optional, so U115 and U116 may not be added. Check supply voltages only.

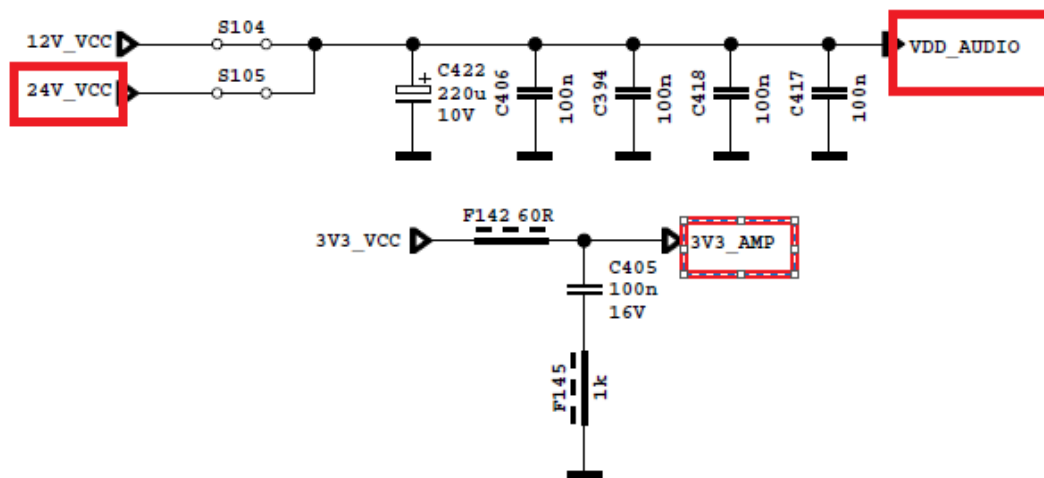
USB1&2 2.0



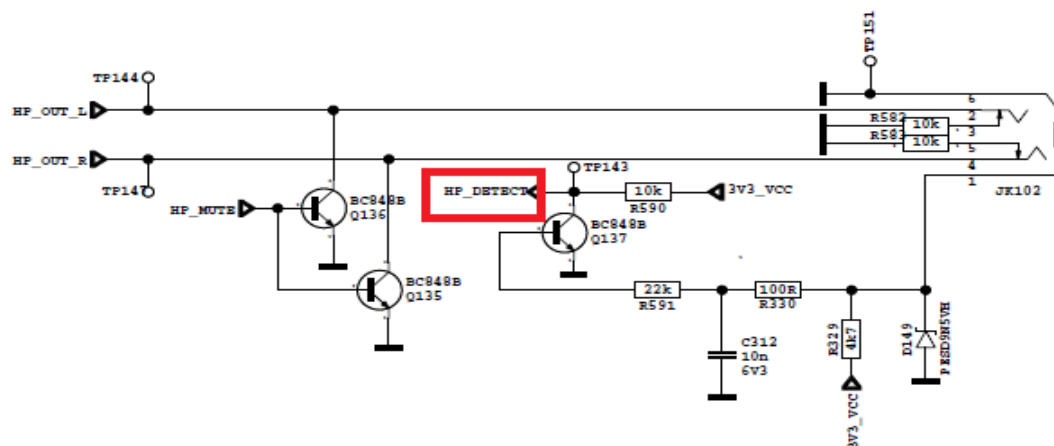
E. NO SOUND PROBLEM

Problem: No audio at main TV speaker outputs.

Check supply voltages of 24V_VCC, VDD_AUDIO and 3V3_AMP with a voltage-meter. There may be a problem in headphone connector or headphone detect circuit. Measure voltage at HP_DETECT pin, it should be 3.3v.



HEADPHONE OUTPUT



F. STANDBY ON/OFF PROBLEM

Problem: Device cannot boot, TV hangs in standby mode.

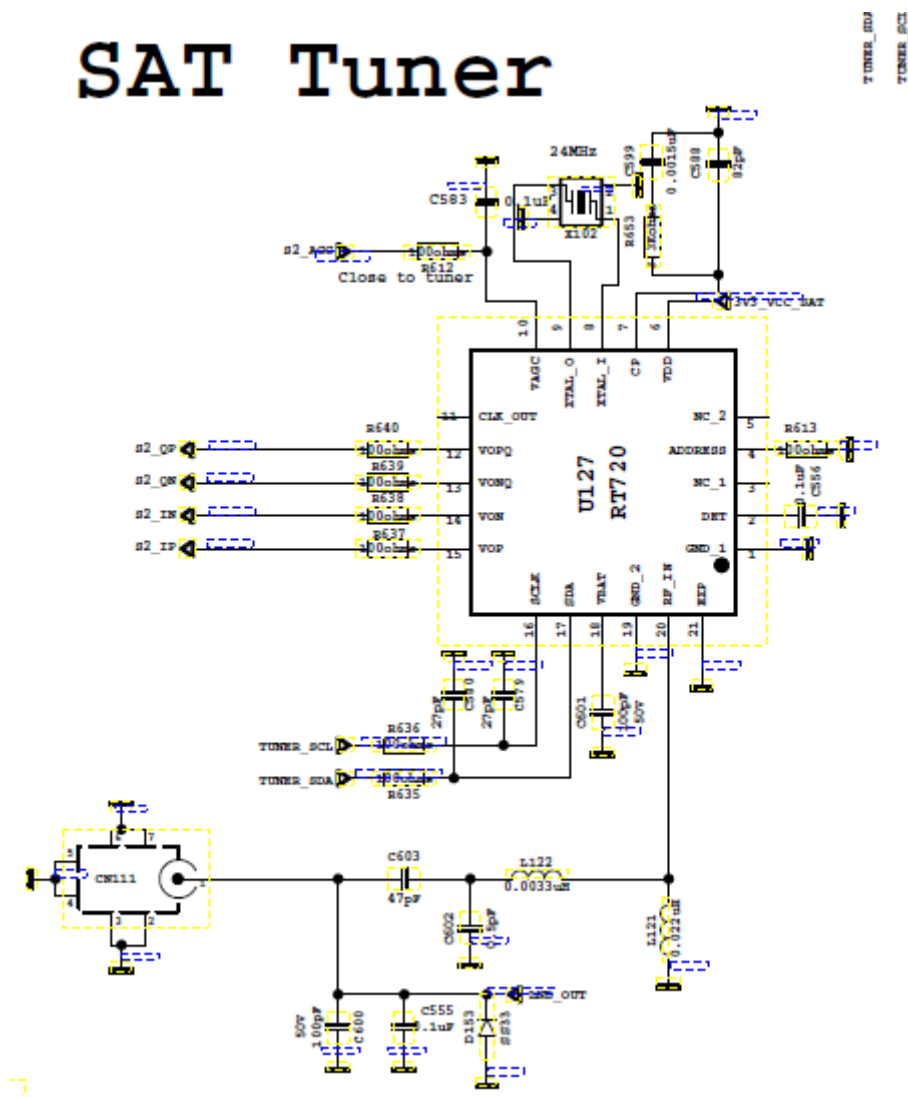
There may be a problem about power supply. Check main supplies with a voltage-meter. Also there may be a problem about SW. Try to update TV with latest SW. Additionally it is good to check SW printouts via Teraterm program. These printouts may give a clue about the problem. You can use HDMI1 for Teraterm program connection.

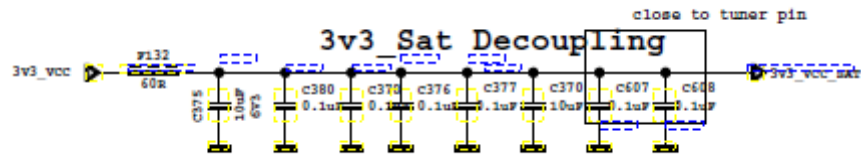
G. NO SIGNAL PROBLEM

Problem: No signal or Low signal in DVB-S/S2 mode.

Check signal cables and LNB voltage, if there is no problem, check RT720 (U127) supply voltages; 3V3_VCC_SAT.

If the above measurements are OK, then check i2c waveforms and software.





12. SERVICE MENU SETTINGS

In order to reach service menu, first Press “MENU” on remote controller. Then get Speaker>>Balance section. Press “4725” while your marker toggle on Balance section.

You can see the service menu main screen below. You can check SW releases by using this menu. In addition, you can make changes on video, audio etc. by using video settings, audio settings titles.

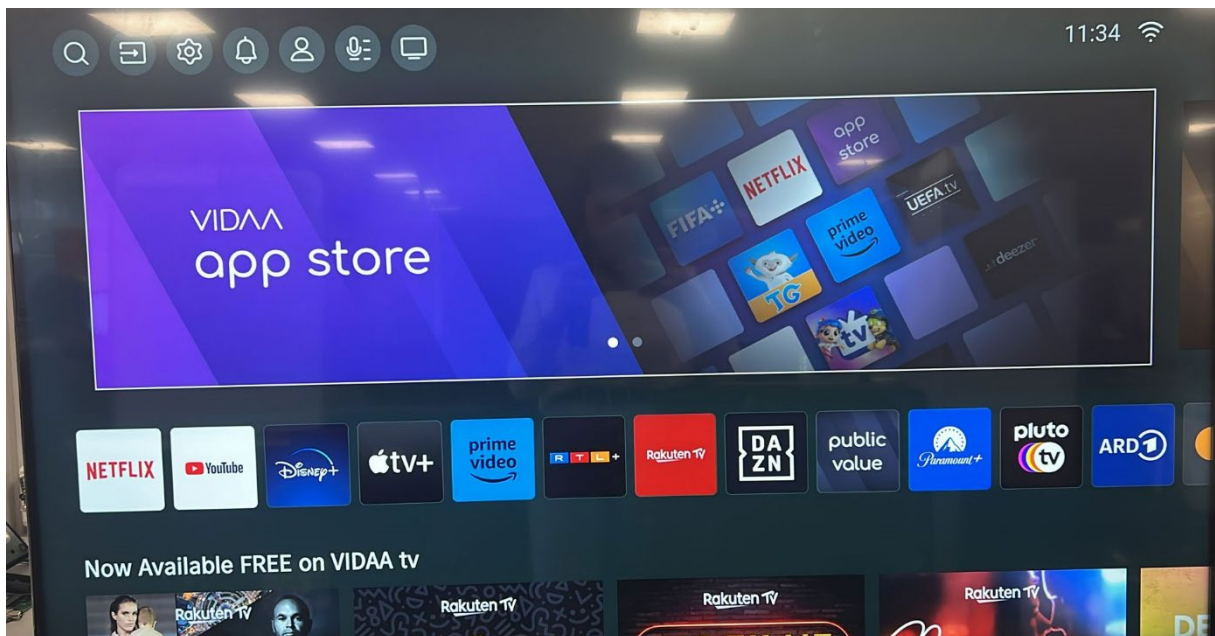


Figure 20: Menu



Figure 21: Video Settings

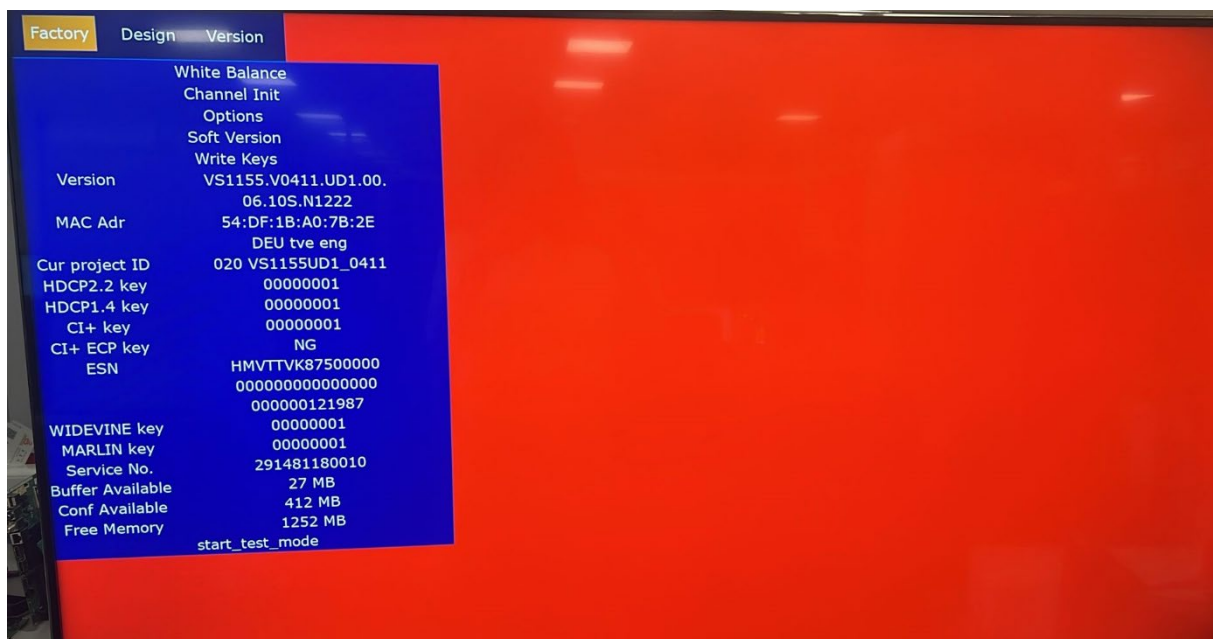


Figure 22: Options 1

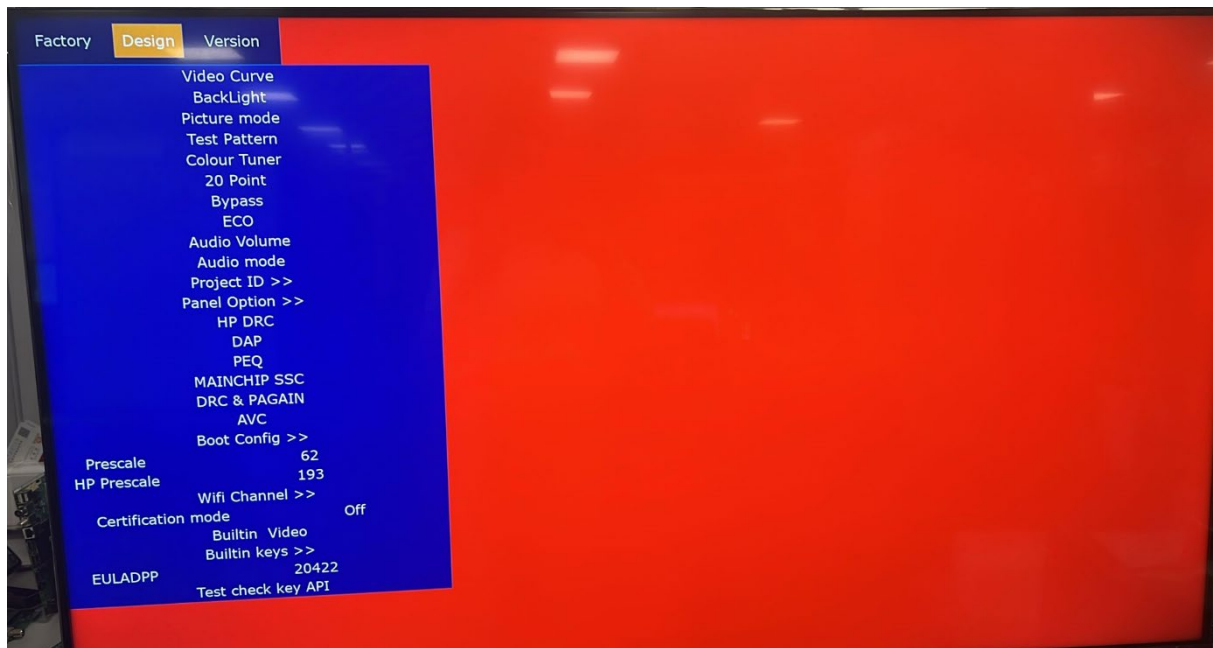


Figure 23: Options 2

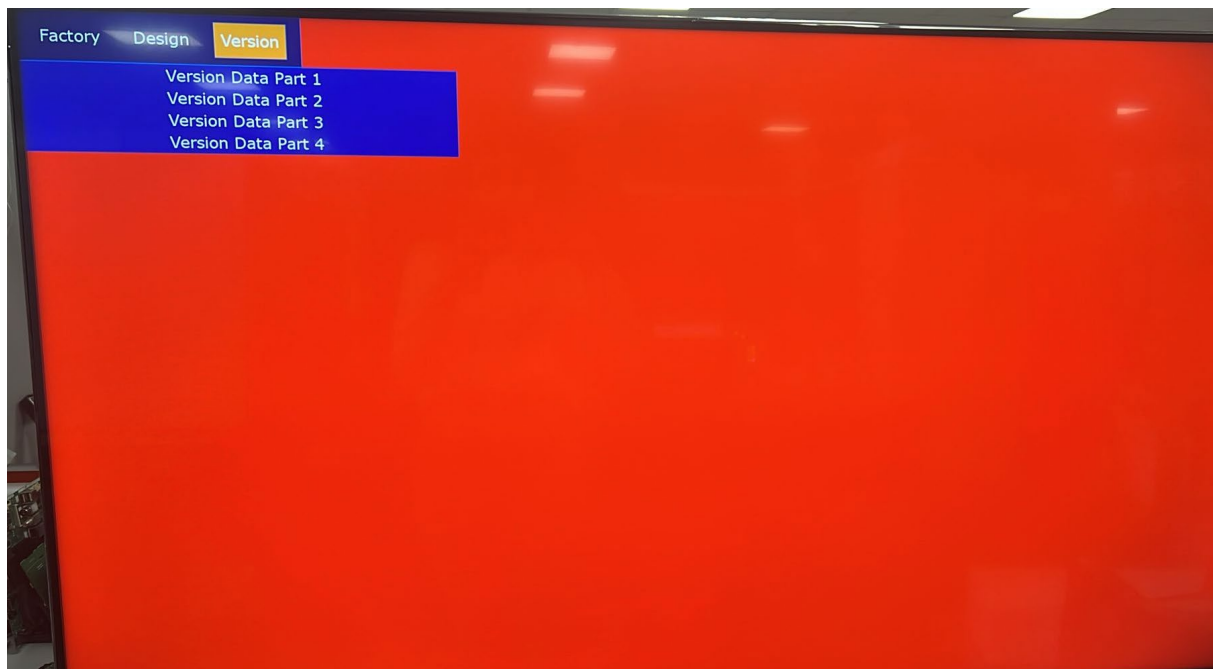
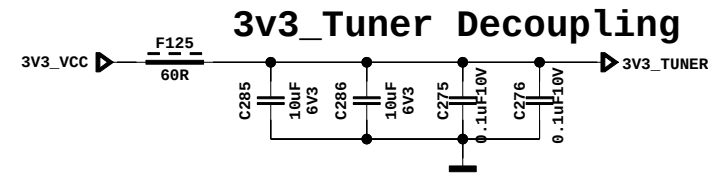
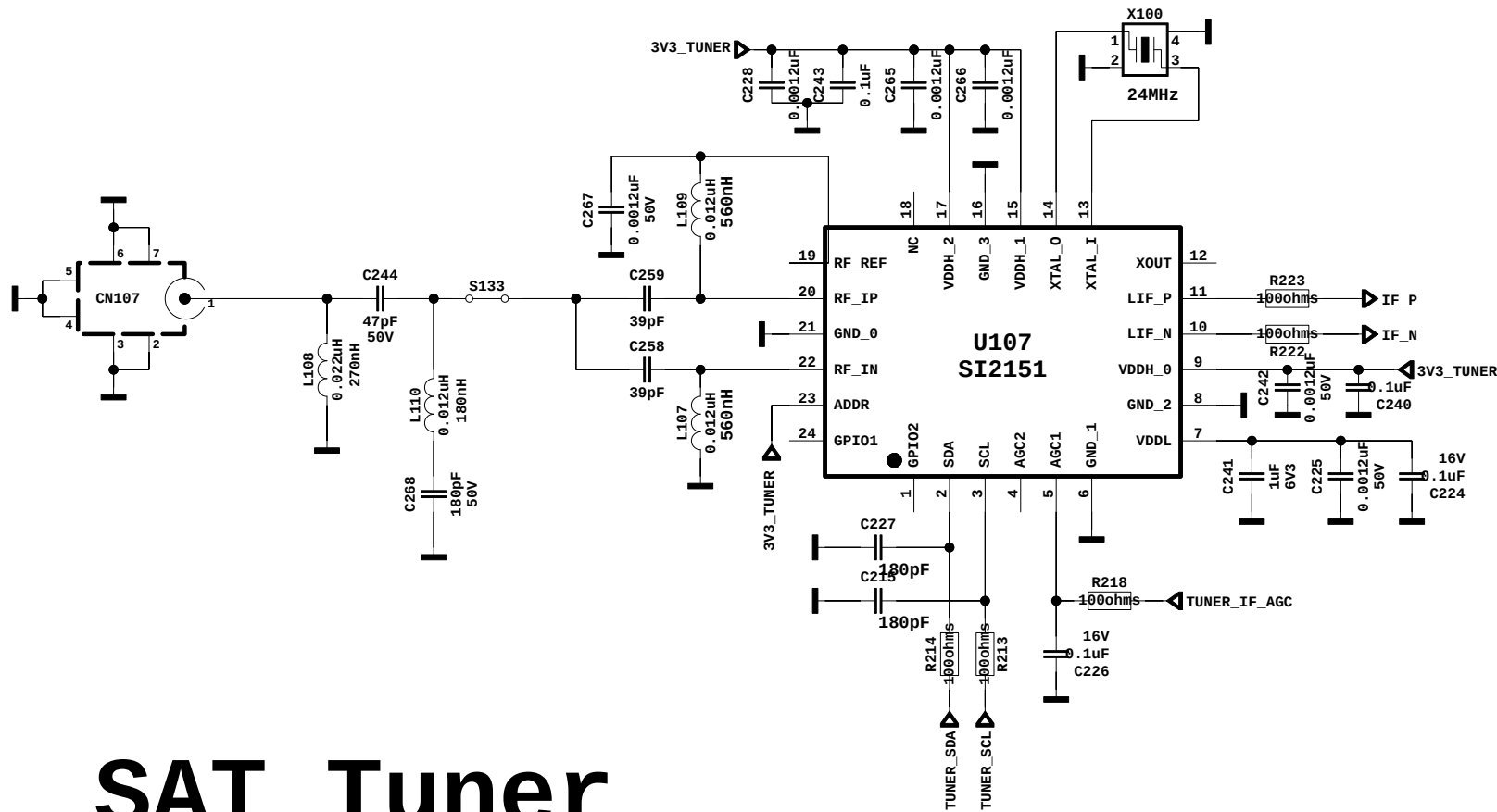
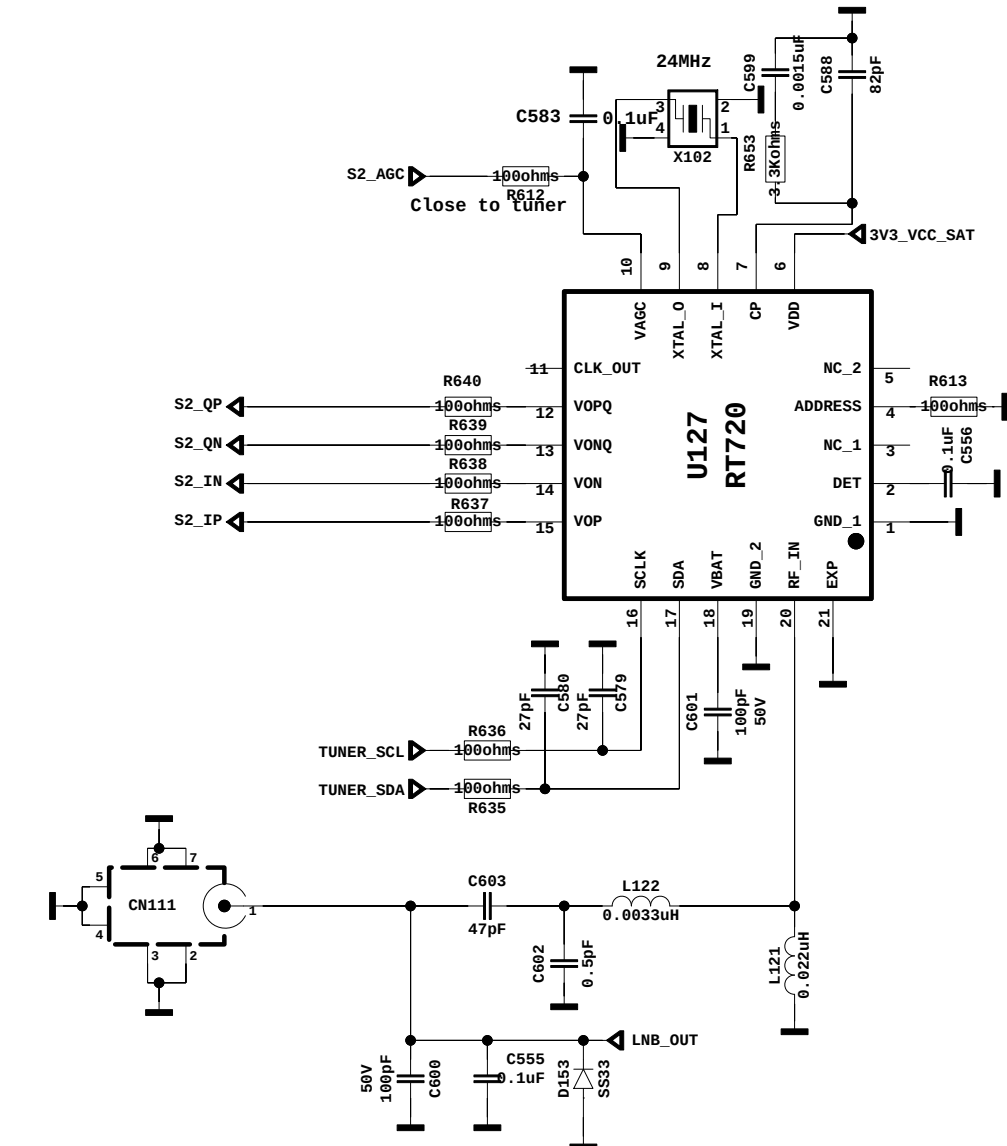


Figure 24: Options 3

Tuner

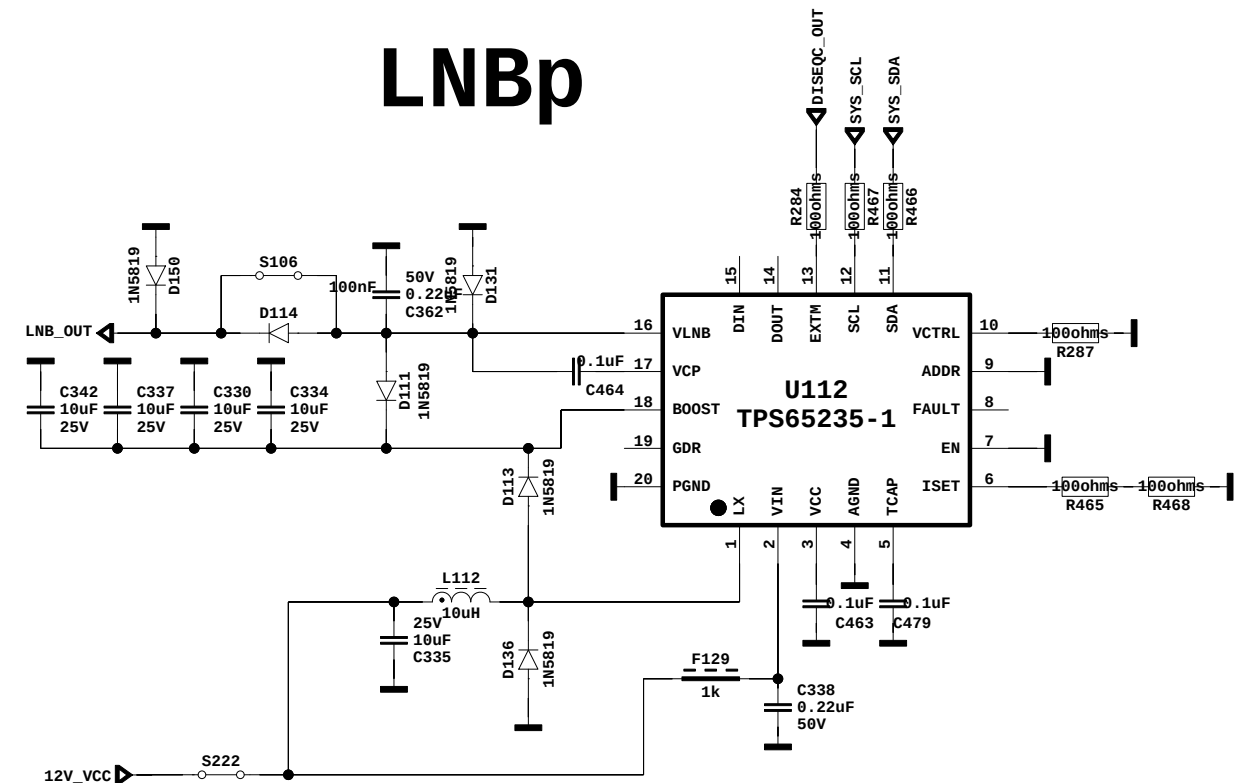


SAT Tuner

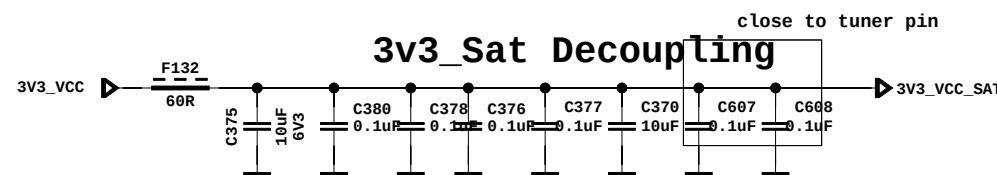


ADDR PIN	I2C ADDRESS
Connected to GND	0x34
27Kohm	0x74
56Kohm	0xB4
120Kohm	0xF4

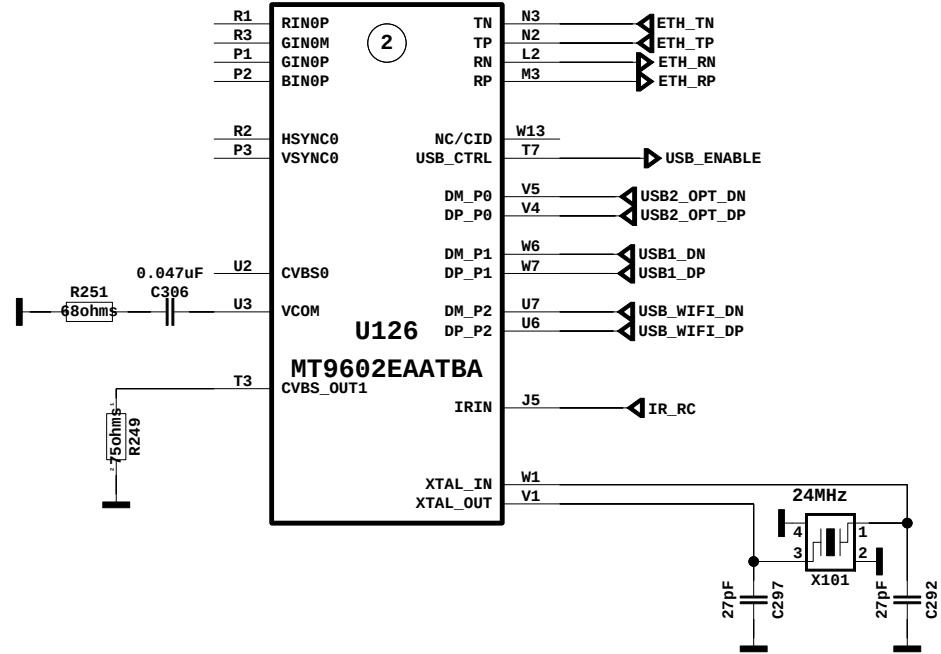
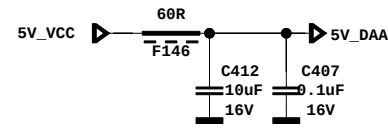
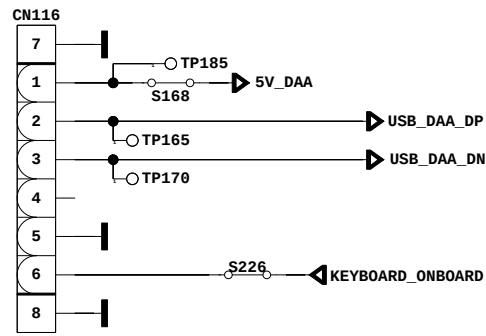
LNBp



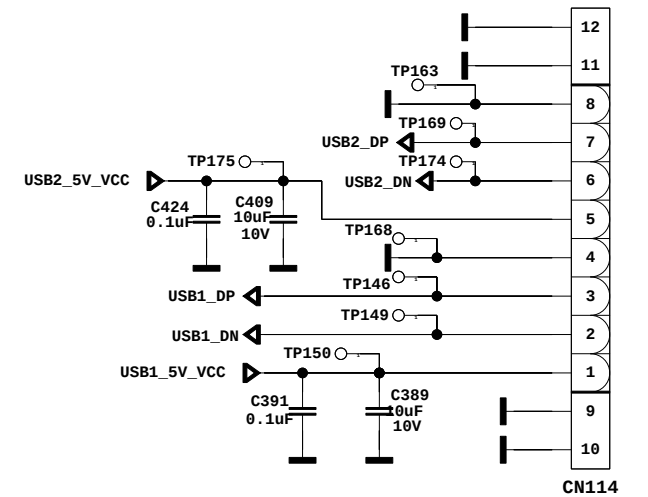
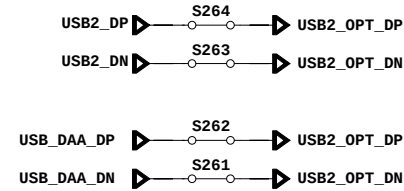
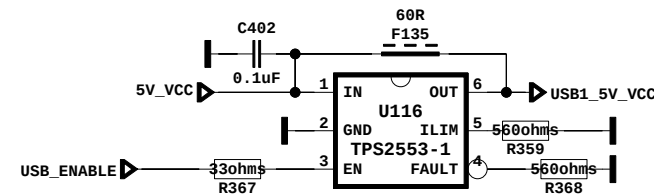
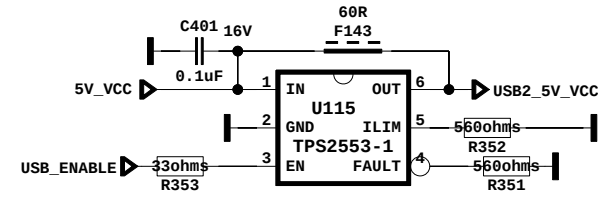
3v3_Sat Decoupling



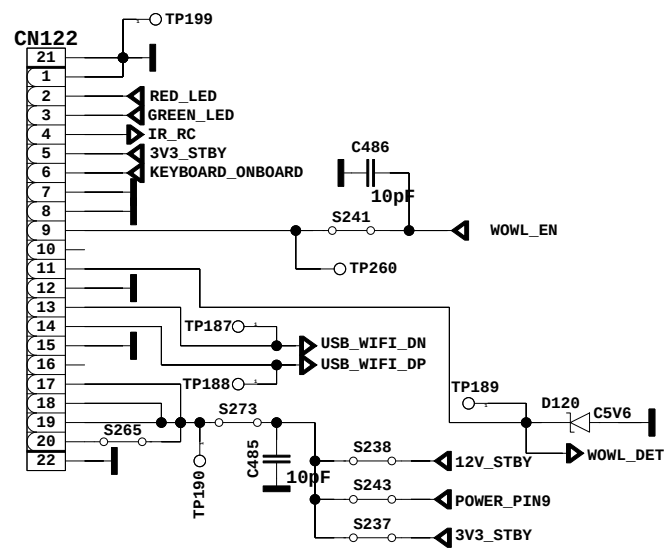
DAA INTERFACE

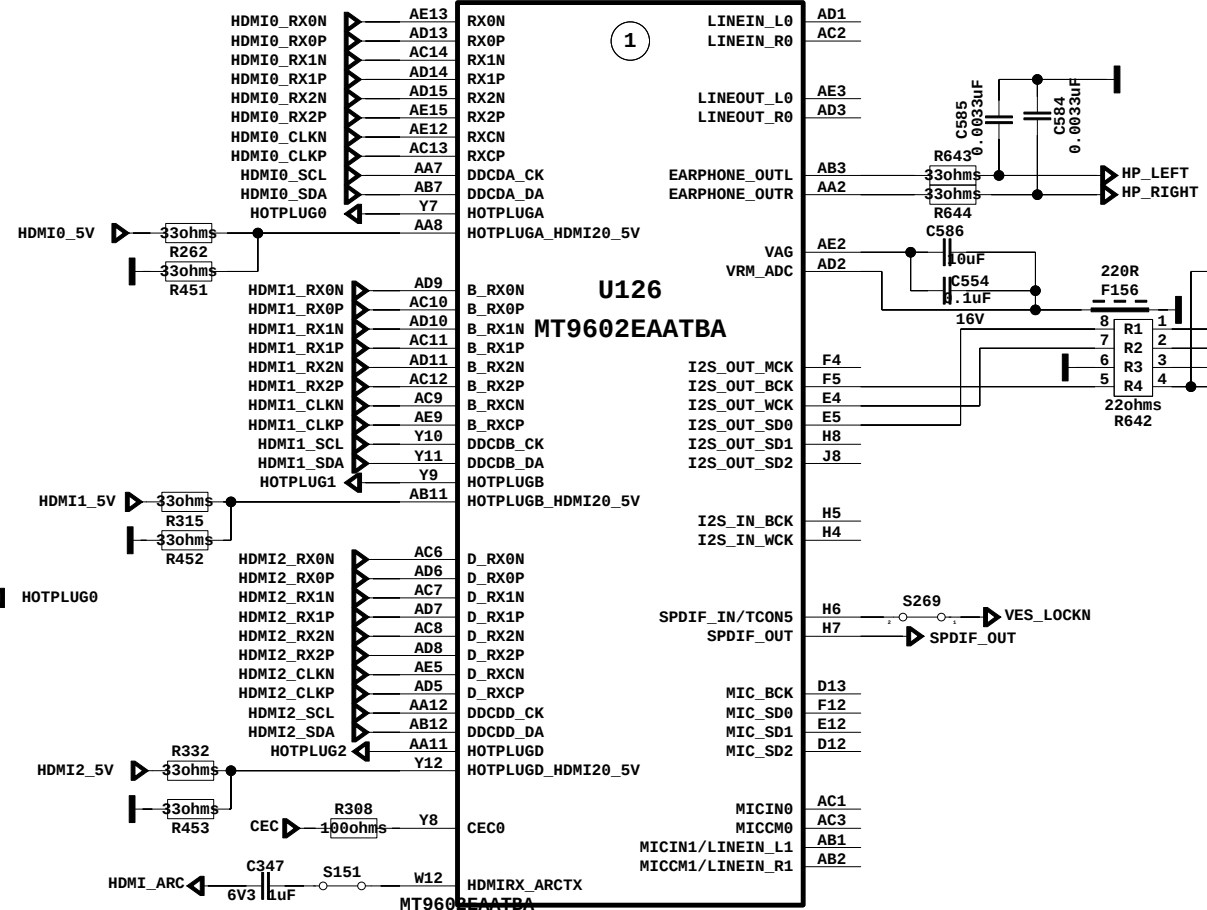


USB1&2 2.0



WIFI&BT&LED_IR





CN112

Pin	Signal
2	ETH_TP
3	ETH_TN
4	ETH_RP
5	ETH_RN
1	TCT
6	RCT
7	NC1
8	NC2
9	SHLD1
10	SHLD2

[illegible]

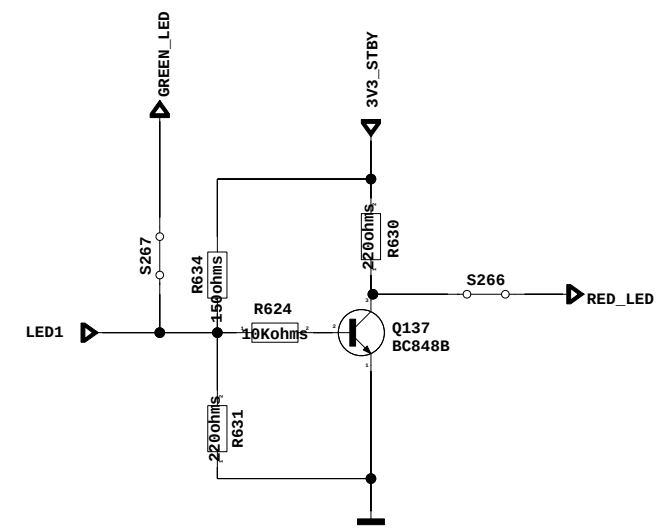
The schematic diagram illustrates the keyboard circuit. It features a 3V3_STBY supply connected to a 10Kohms resistor R342. The other end of R342 is connected to the KEYBOARD_ONBOARD input. The circuit also includes a 47ohms resistor R341, a 1k resistor F133, a 1N5819 diode D125, a 1N5819 diode D137, and a 0.1uF capacitor C390. The KEYBOARD output is connected to the KEYBOARD_ONBOARD input.

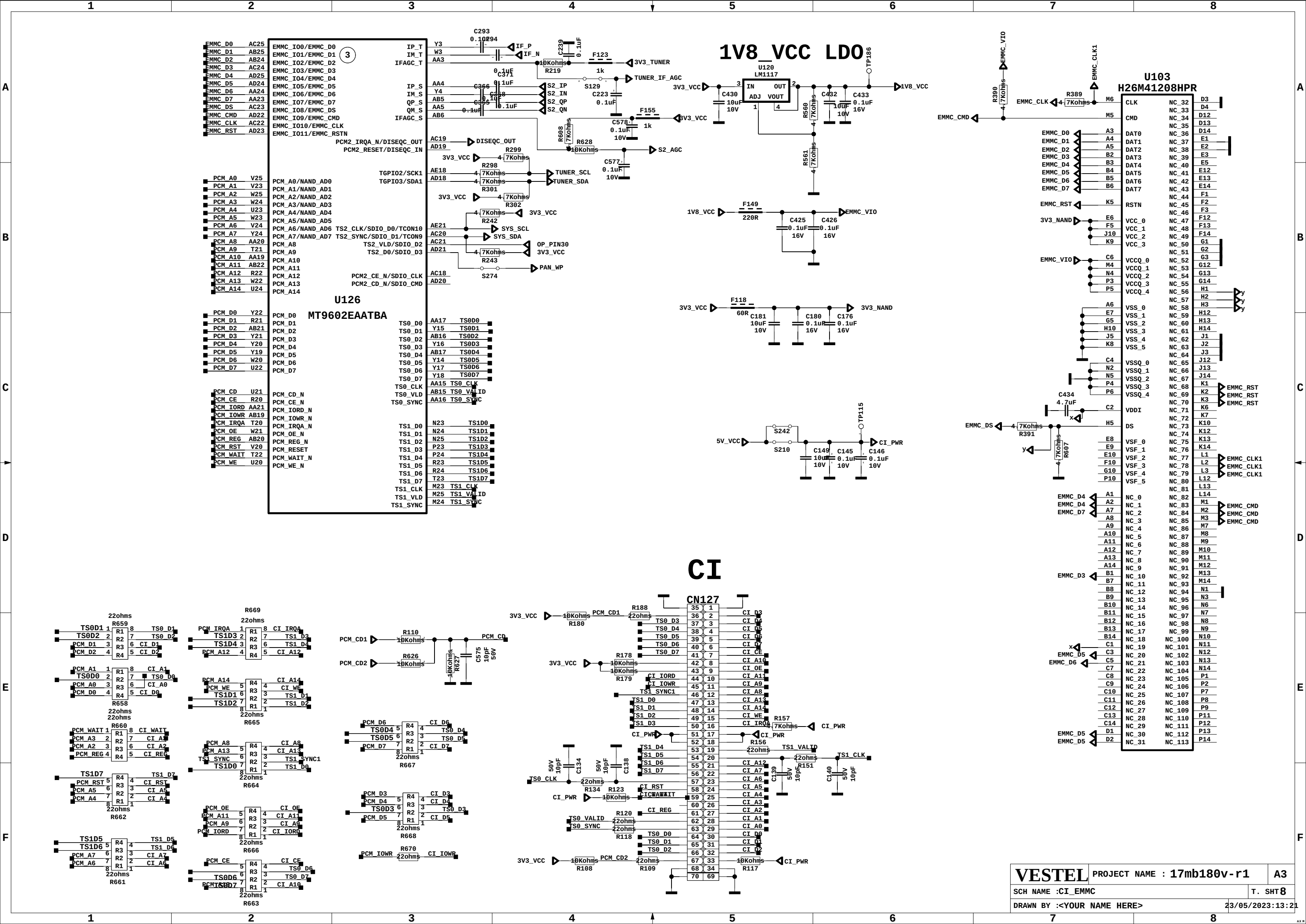
CN113

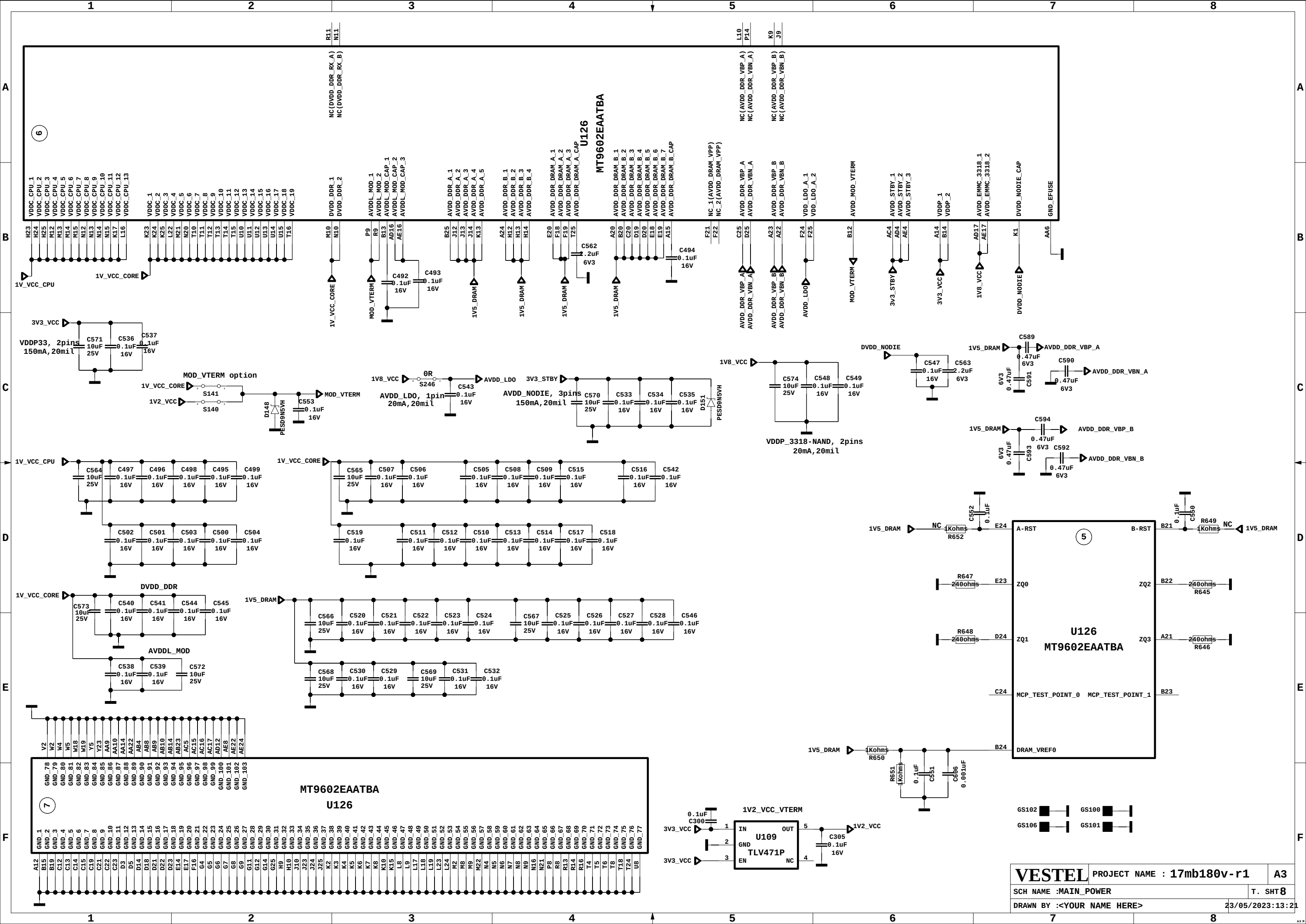
Pin	Signal	Component	Value
1	HDMI2_RX2P		
2	HDMI2_RX2N		
3	HDMI2_RX1P		
4			
5			
6	HDMI2_RX1N		
7	HDMI2_RX0P		
8			
9	HDMI2_RX0N		
10	HDMI2_CLKP		
11			
12	HDMI2_CLKN		
13	CEC		
14	HDMI2_SCL	P271	330ohms
15	HDMI2_SDA	P271	330ohms
16			
17			
18			
19			
20			
21			
22			
23			

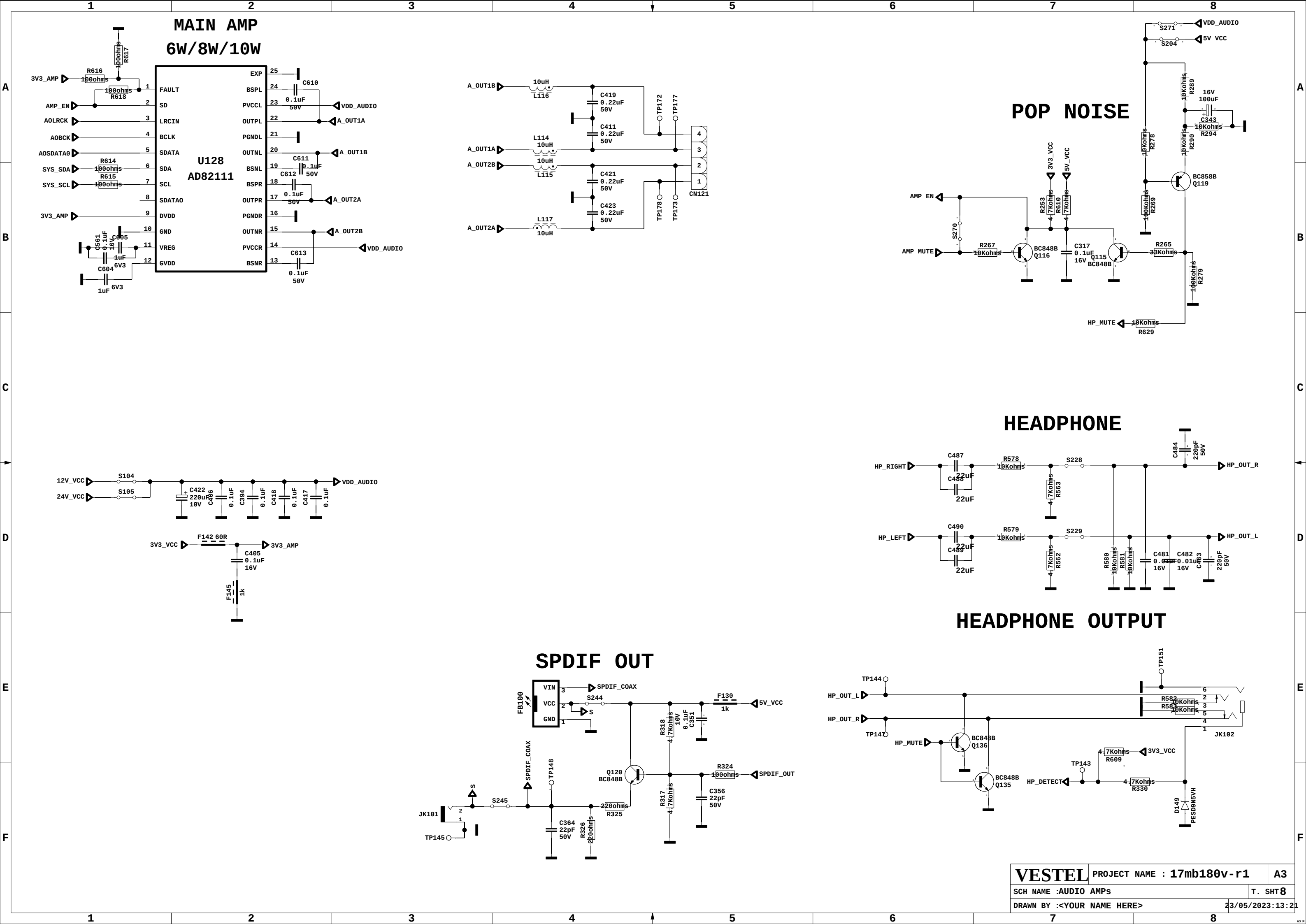
Components:

- Resistors:** R277 (470ohms), R335 (330ohms), R336 (47Kohms), R337 (47Kohms), R334 (330ohms), R459 (1Kohms), R446 (10Kohms), R458 (10Kohms), R633 (470ohms).
- Capacitors:** C587 (15pF 50V).
- Transistors:** Q134 (BC848B), Q133 (BC848B), Q132 (BC848B).
- Other:** TP270, TP273, TP272, TP280.

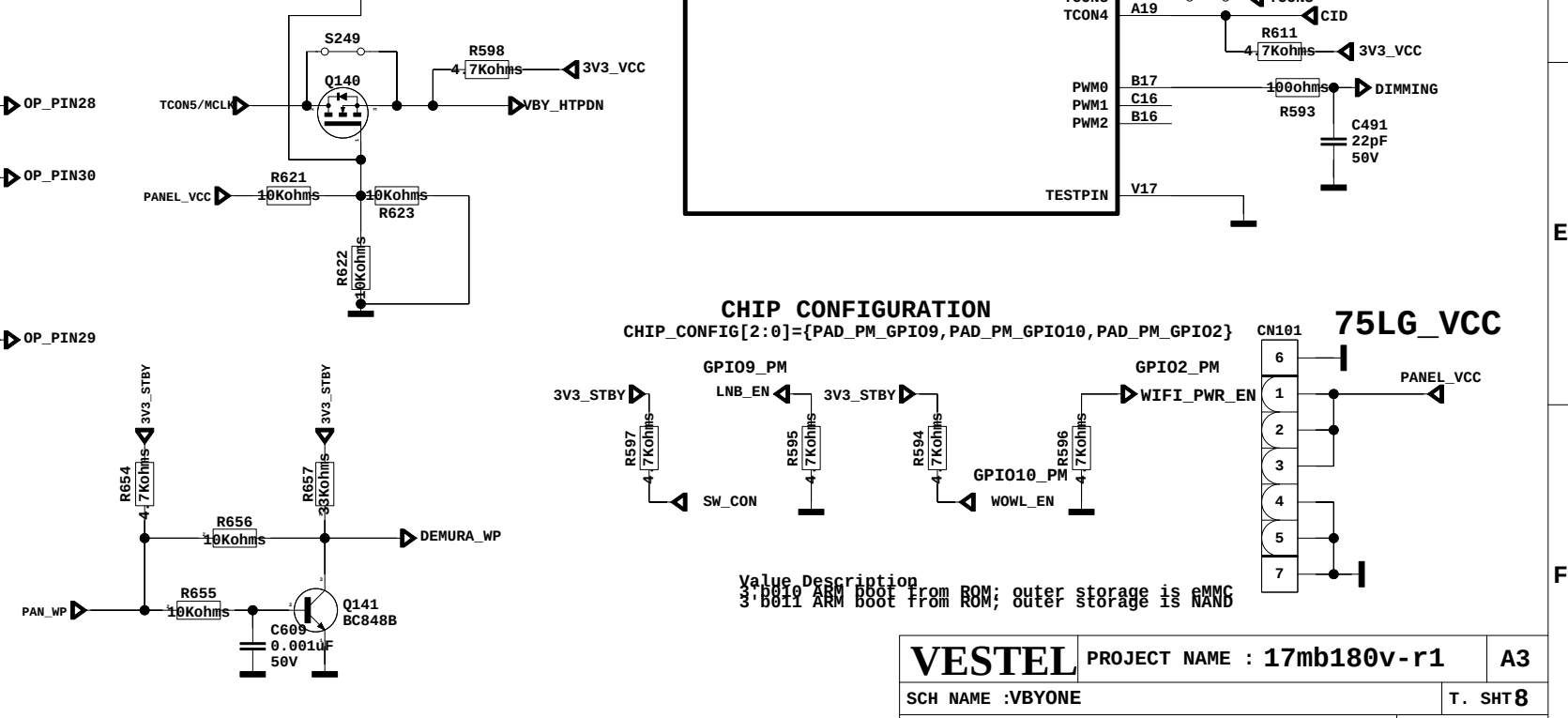
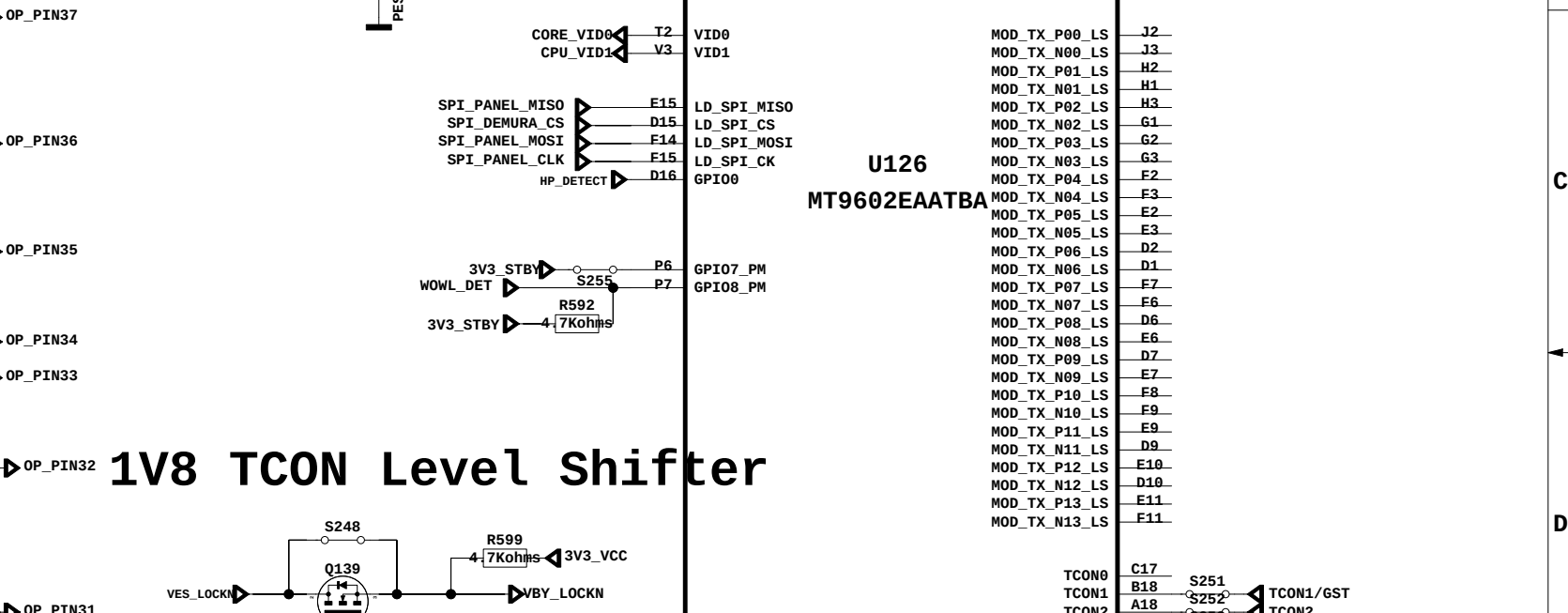
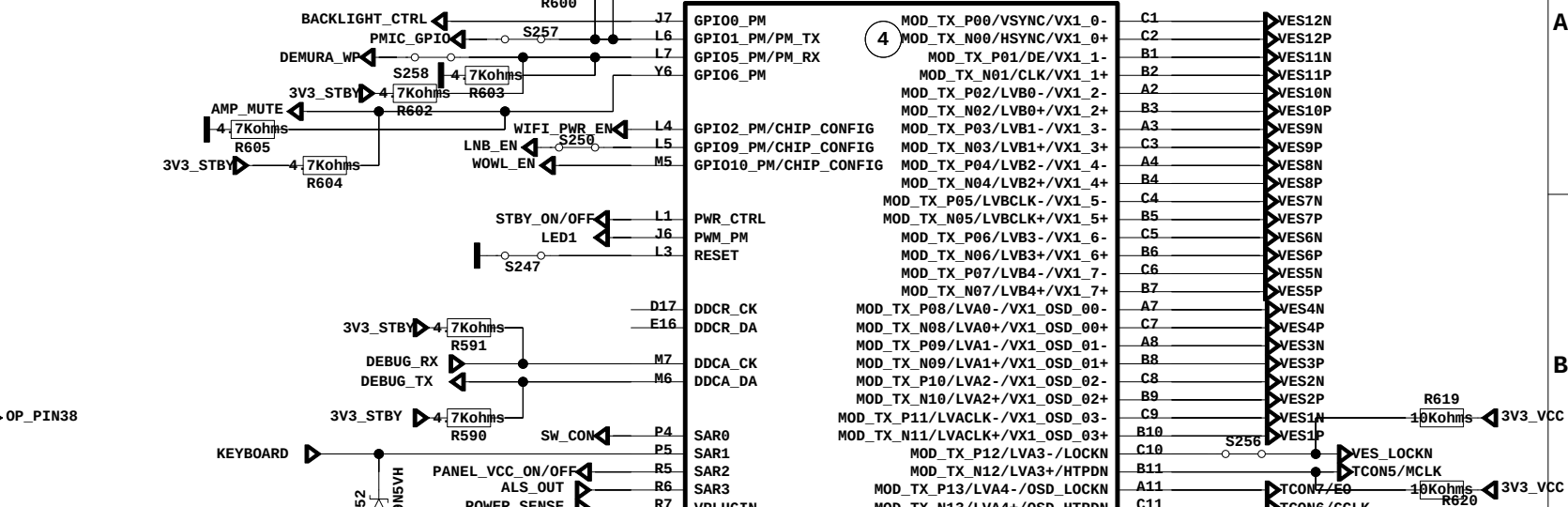
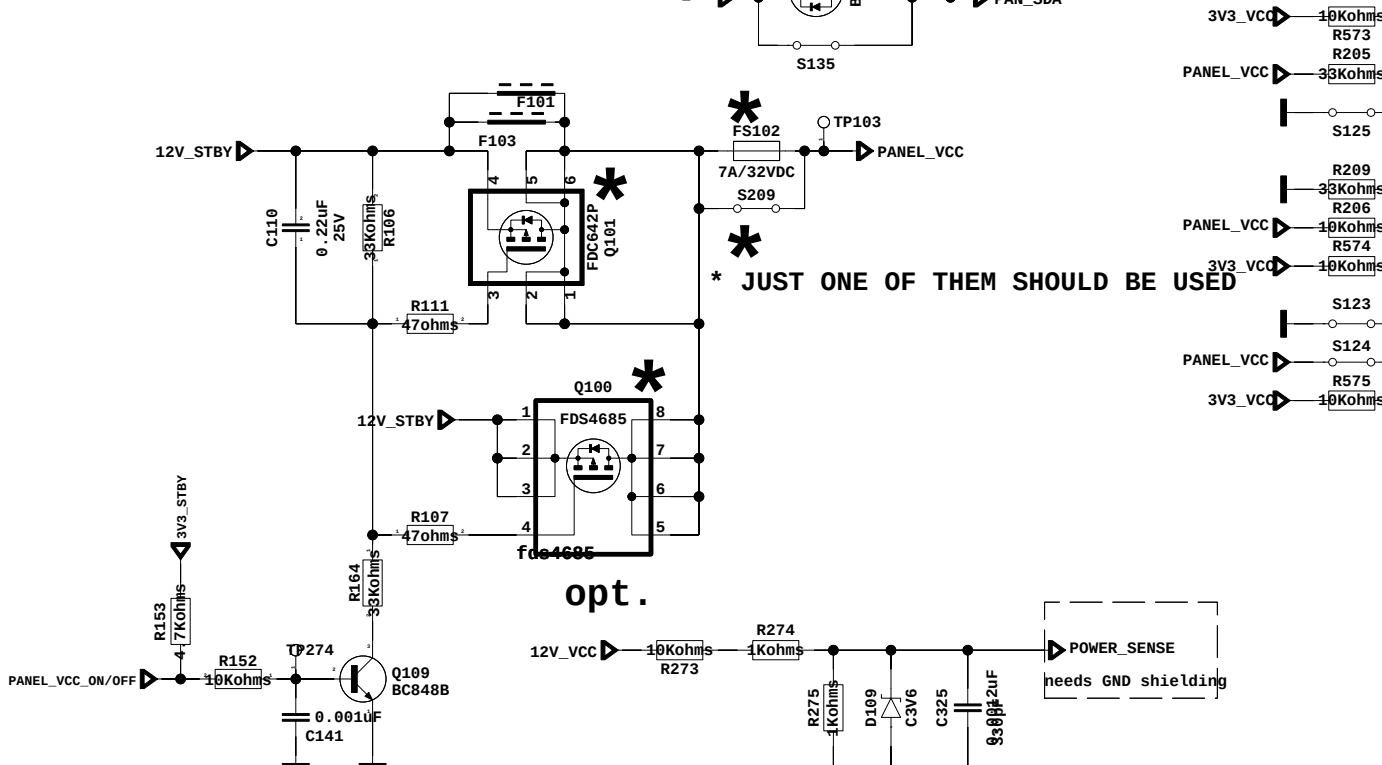
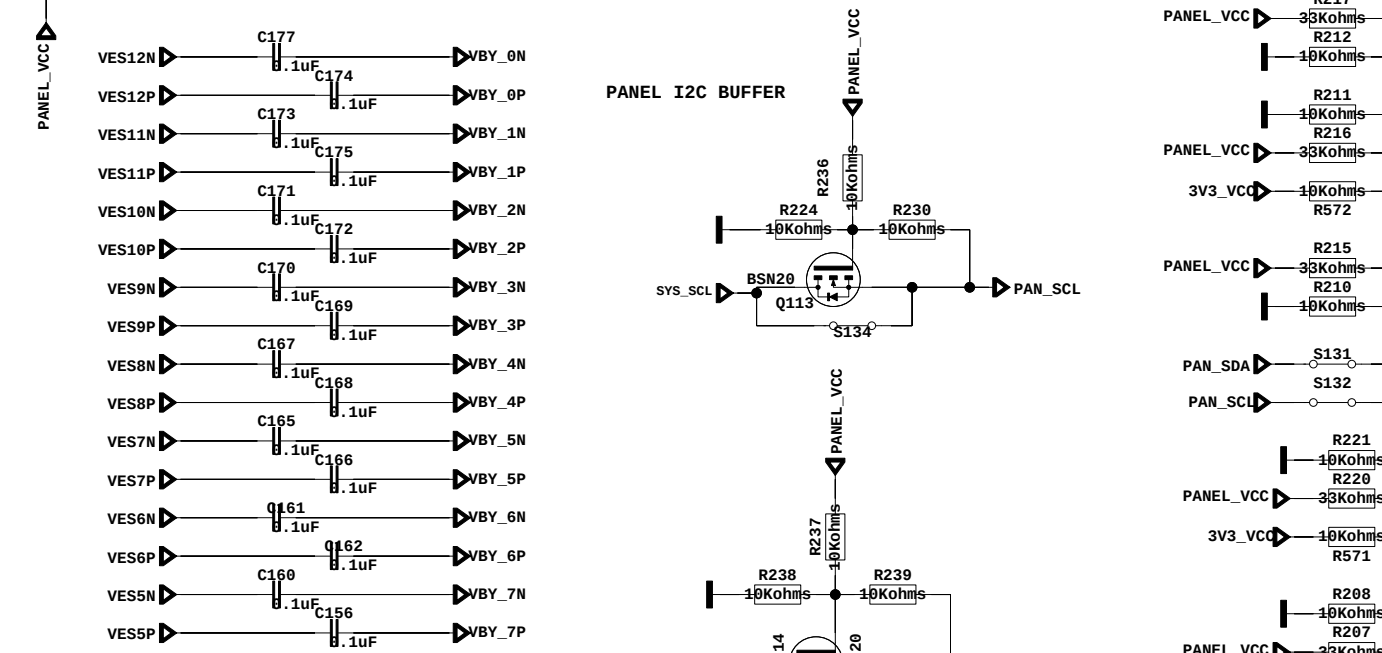
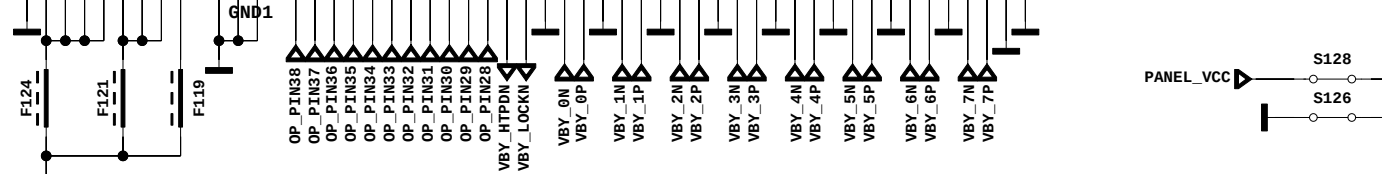
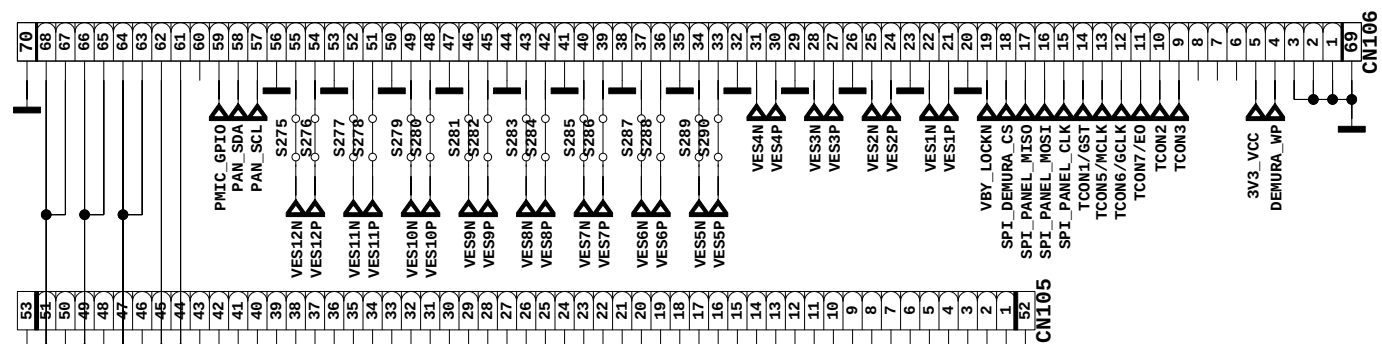




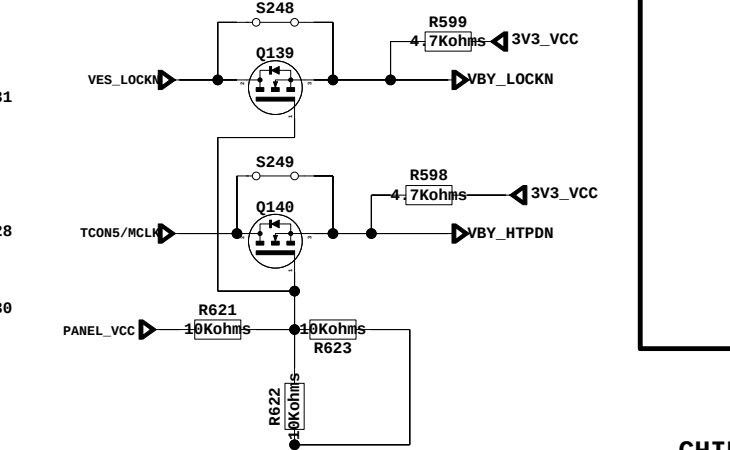




TCONLESS/VBYONE SOCKET

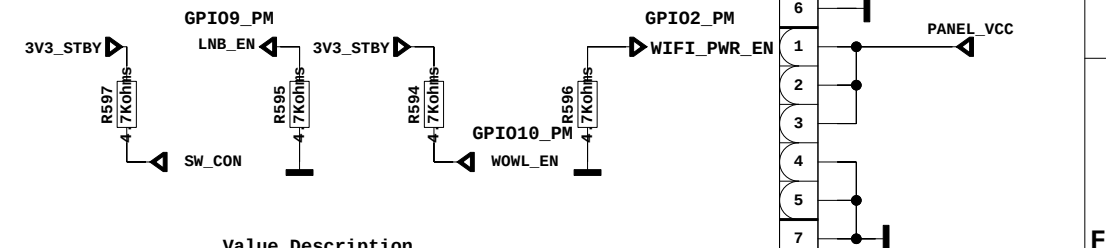


1V8 TCON Level Shifter



CHIP CONFIGURATION

CHIP_CONFIG[2:0]={PAD_PM_GPI09,PAD_PM_GPI010,PAD_PM_GPI02}



Value Description
3:0:011 ARM boot from ROM; outer storage is NVMC

