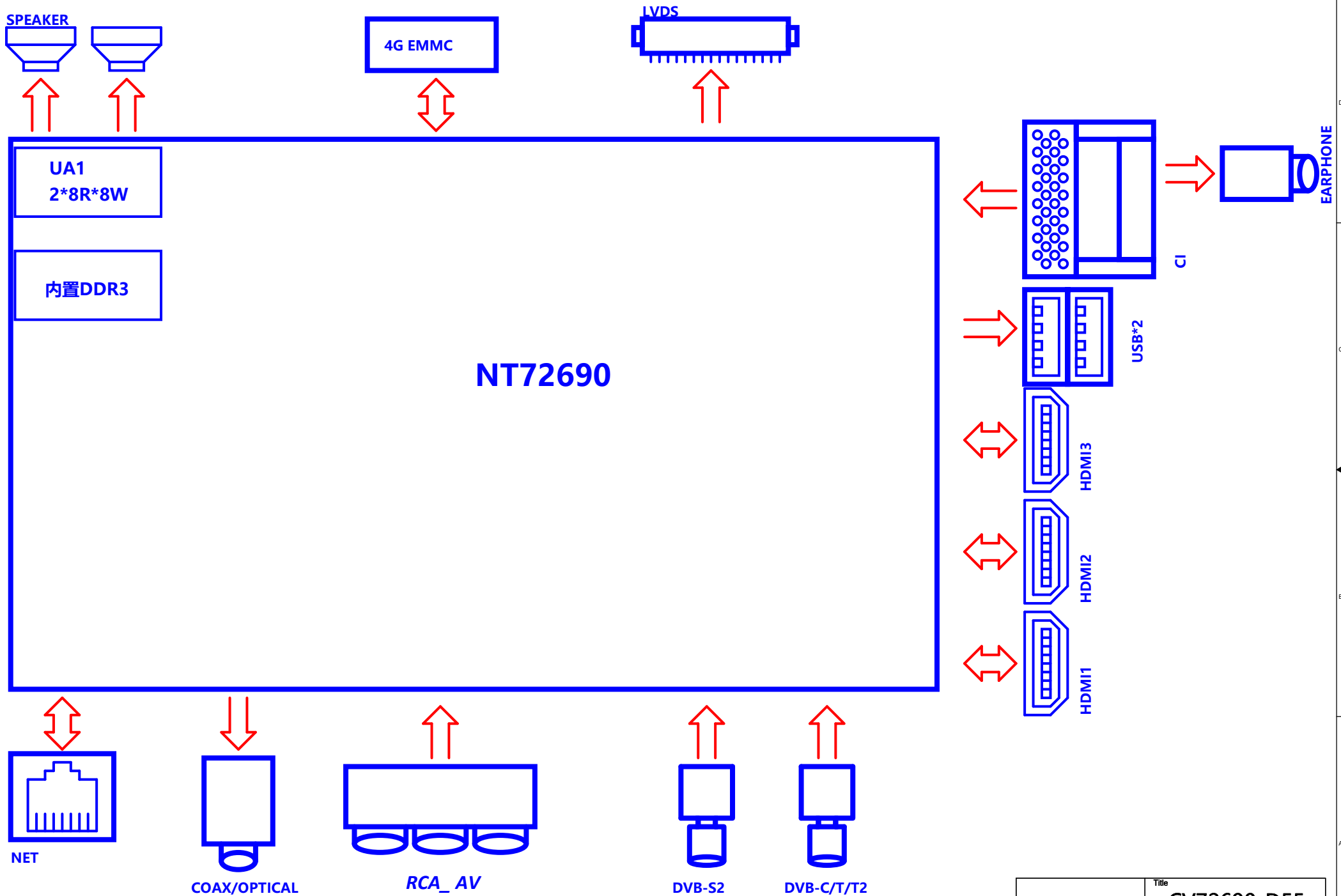
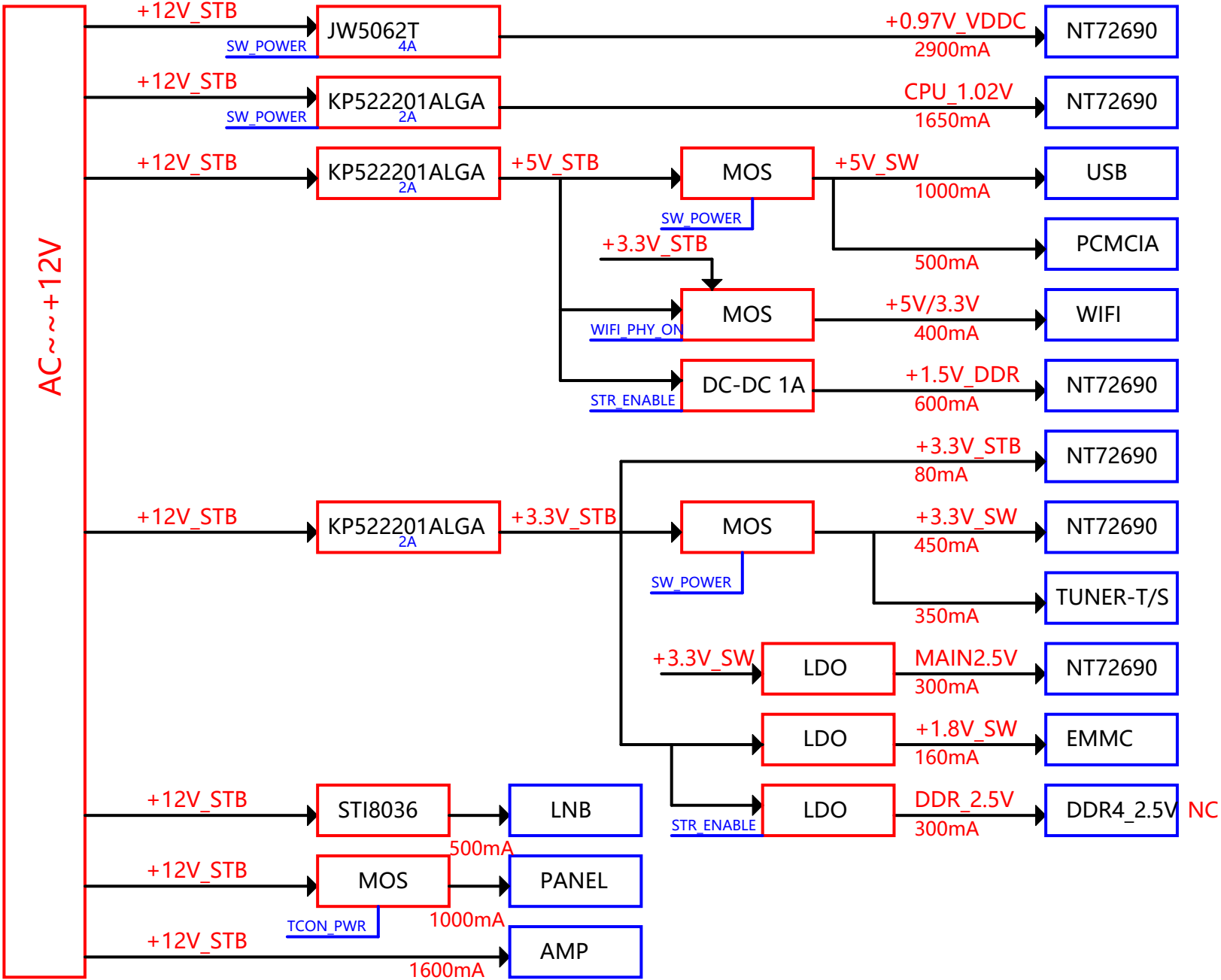
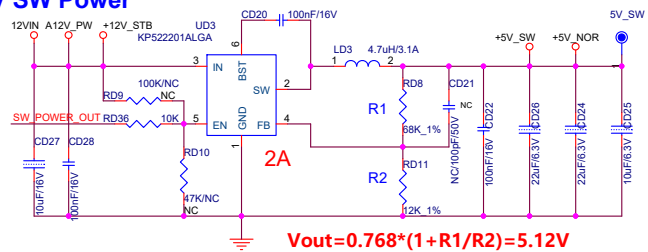




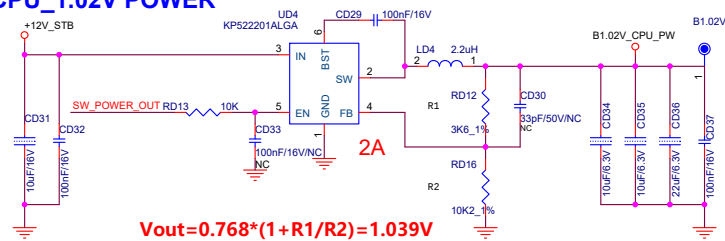
POWER SUPPLY ARCHITECTURE



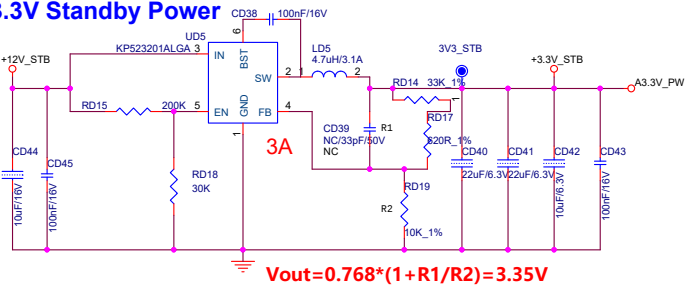
5V SW Power



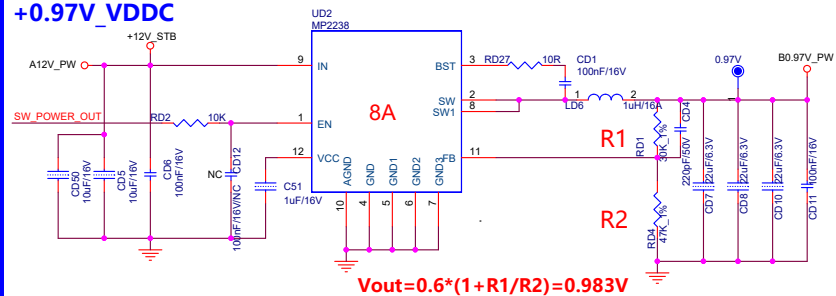
CPU_1.02V POWER



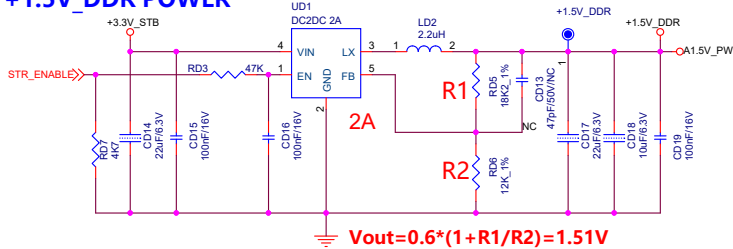
3.3V Standby Power



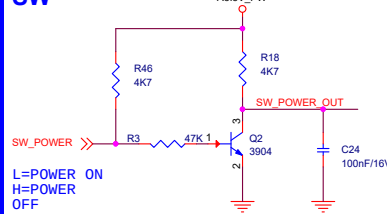
+0.97V_VDDC



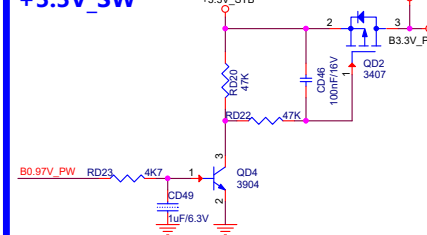
+1.5V_DDR POWER



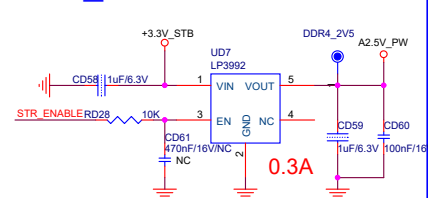
SW



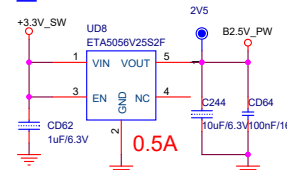
+3.3V_SW



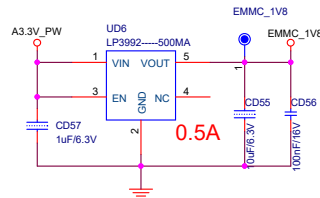
DDR4_2.5V



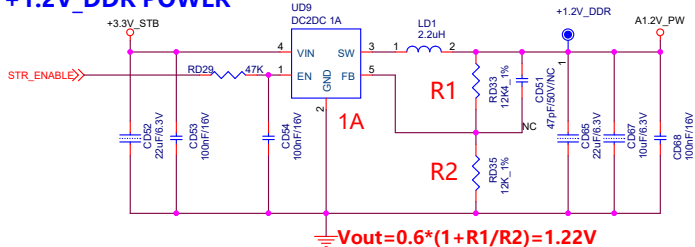
MAIN_2.5V



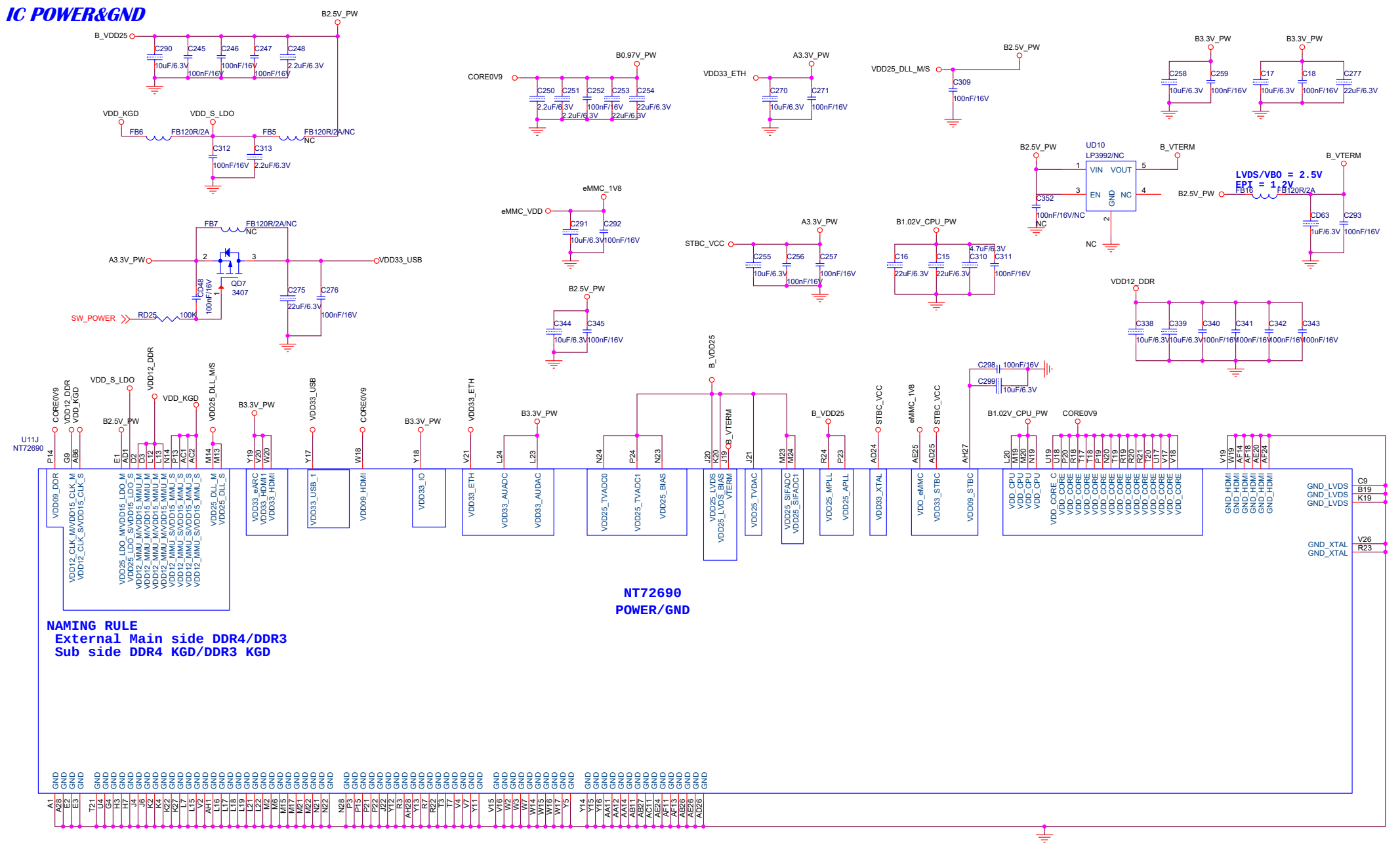
EMMC 1.8V



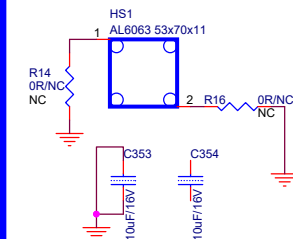
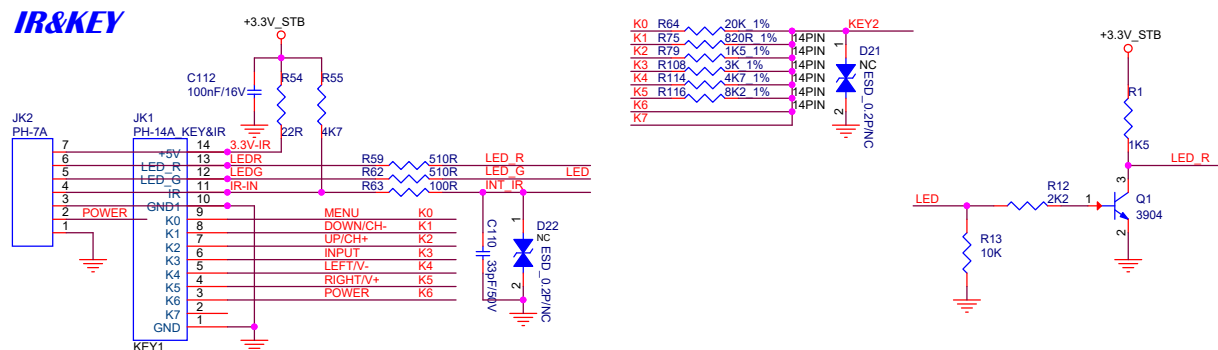
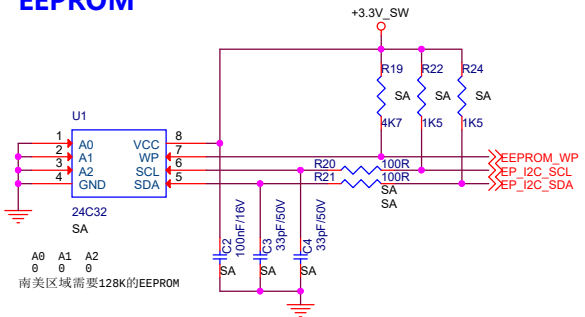
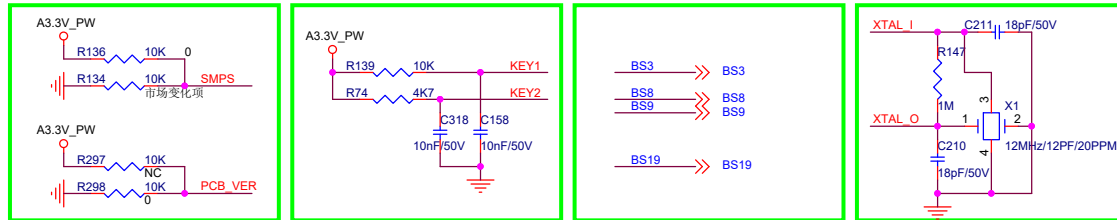
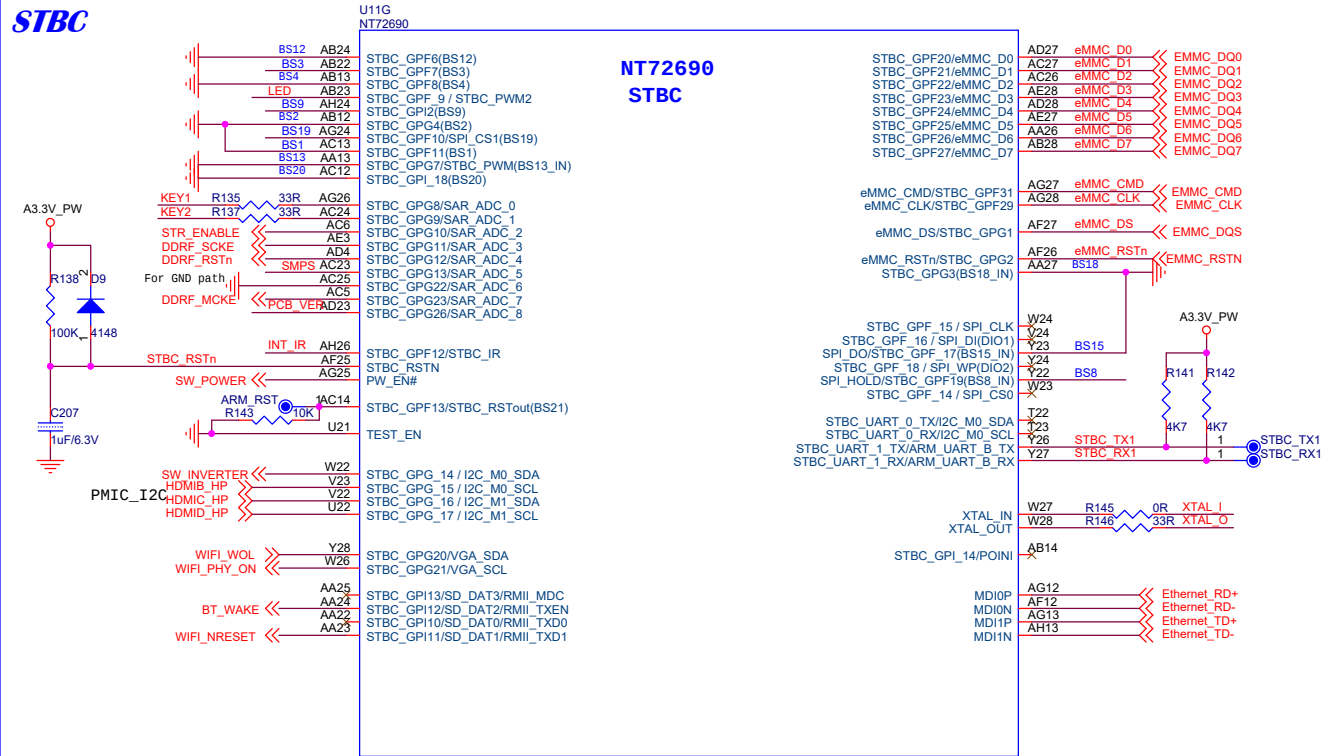
+1.2V_DDR POWER

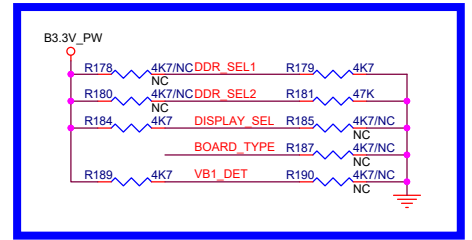
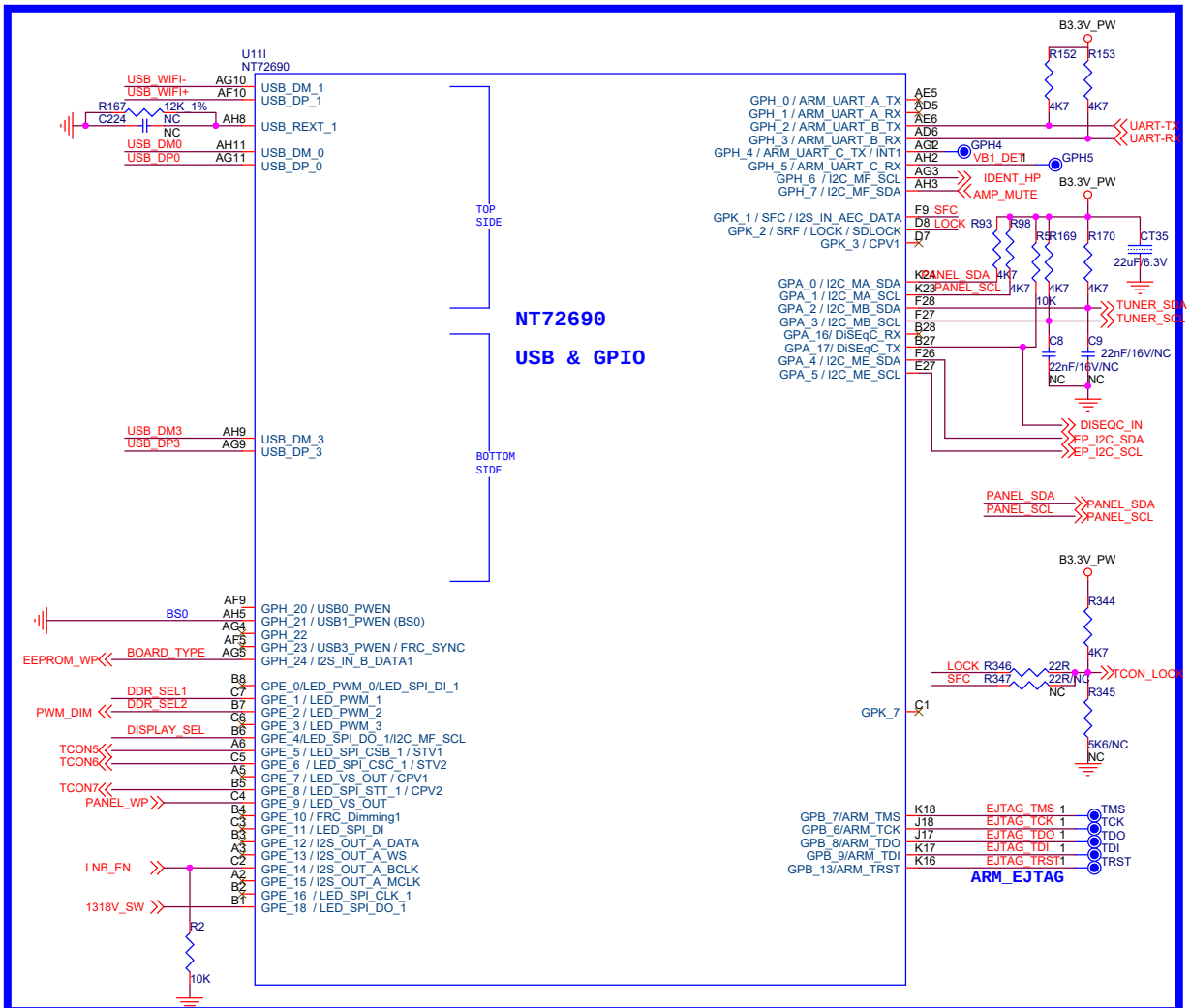
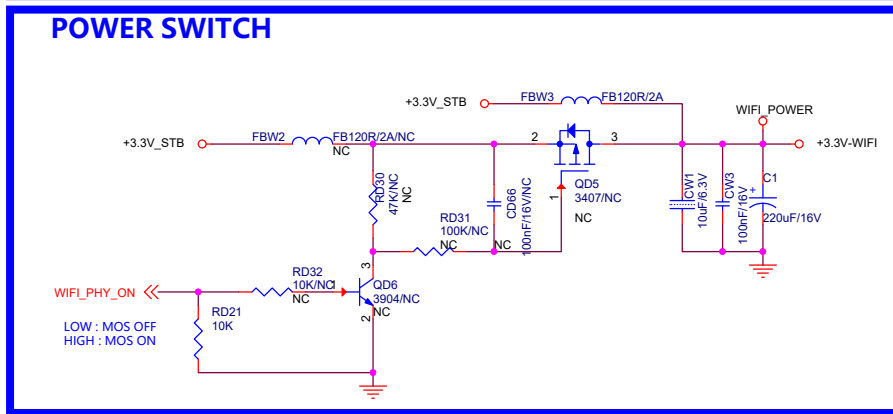
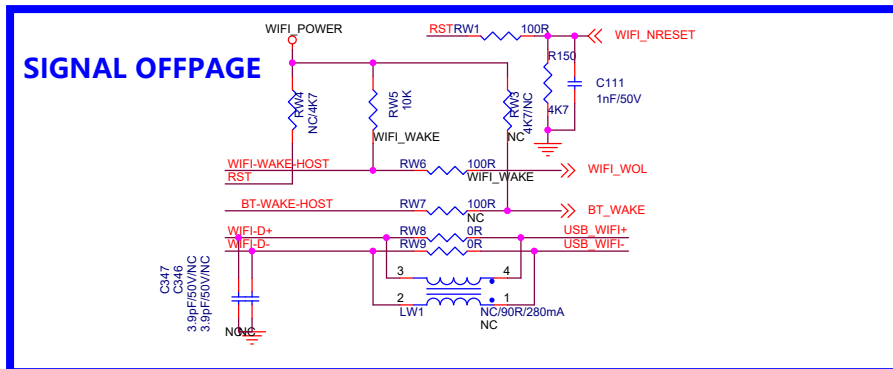
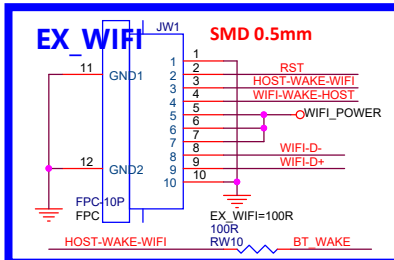
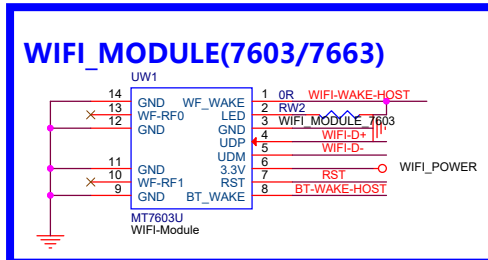
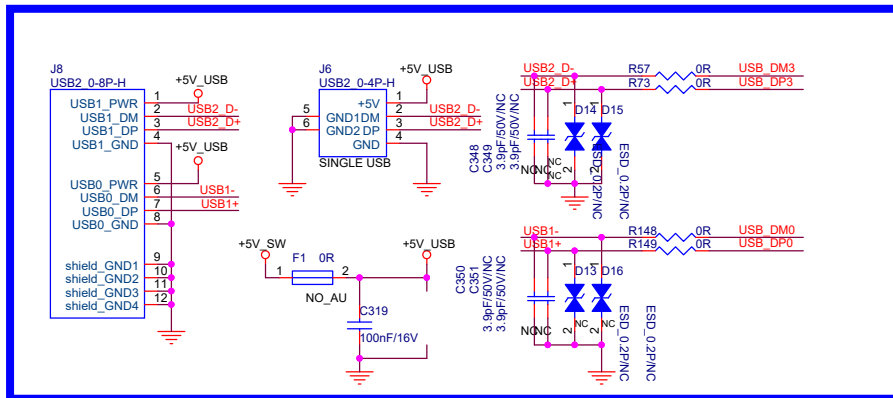


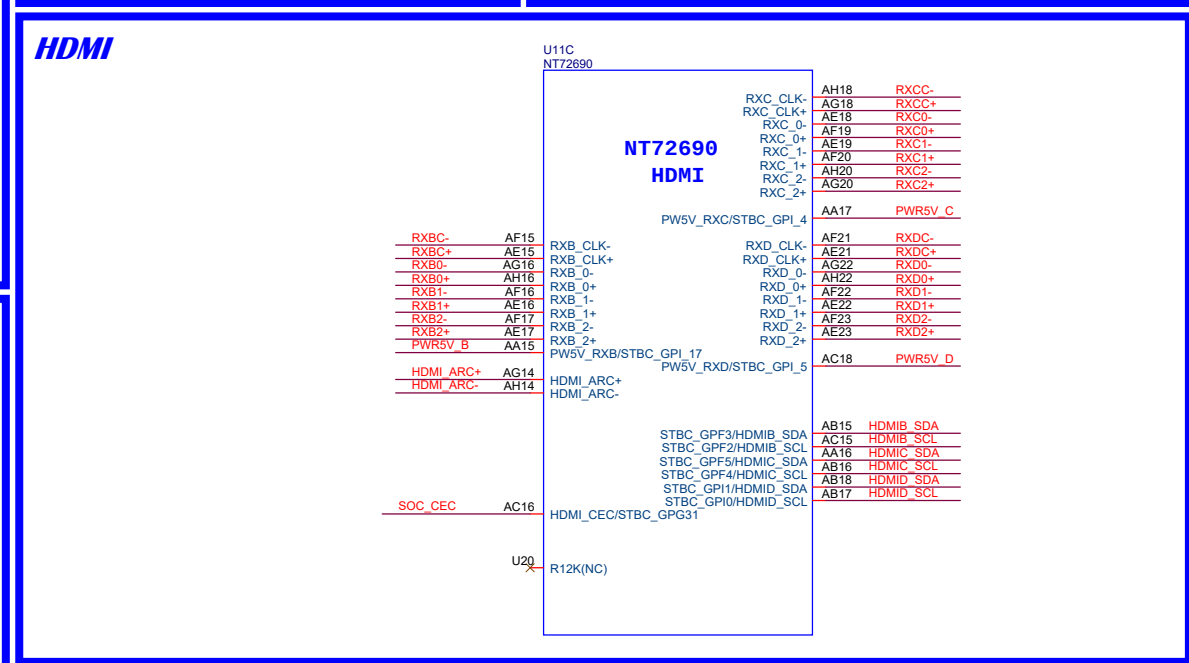
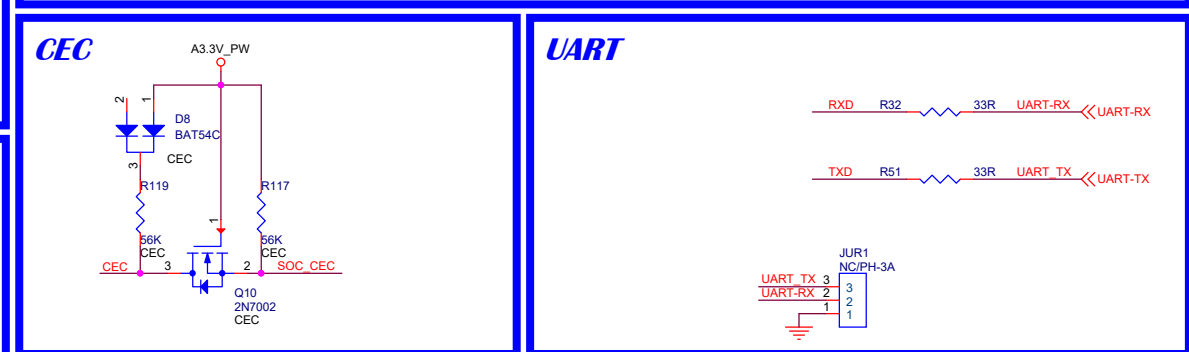
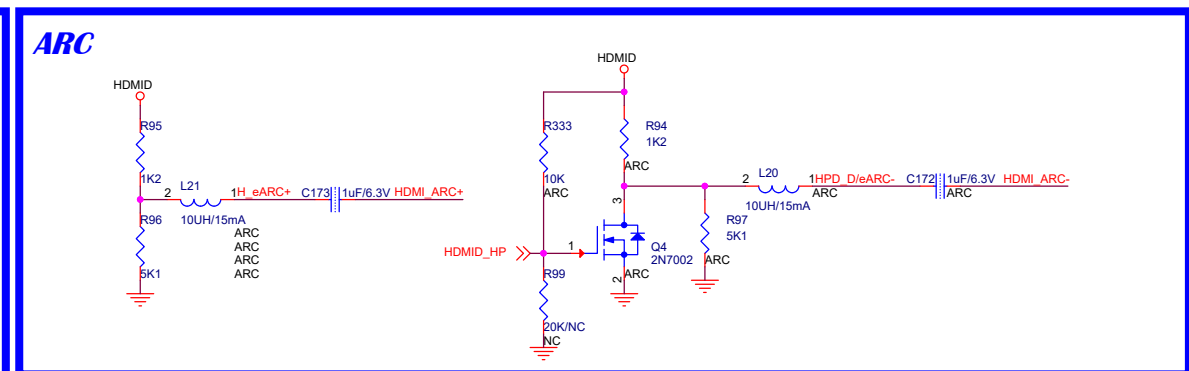
IC POWER&GND



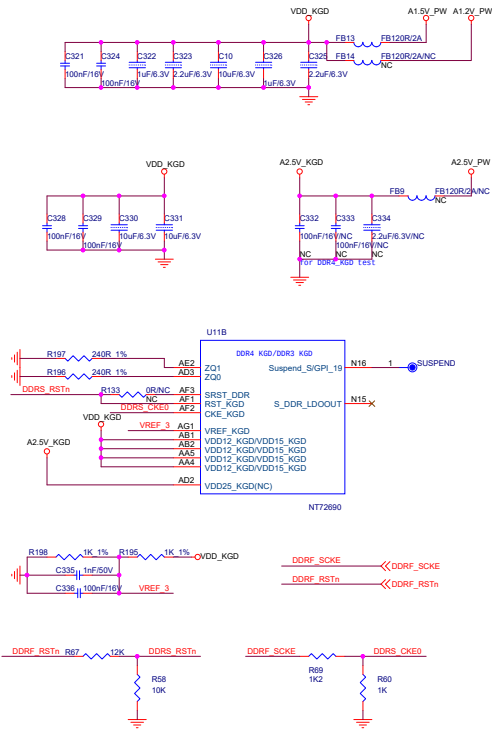
NAMING RULE
External Main side DDR4/DDR3
Sub side DDR4 KGD/DDR3 KGD



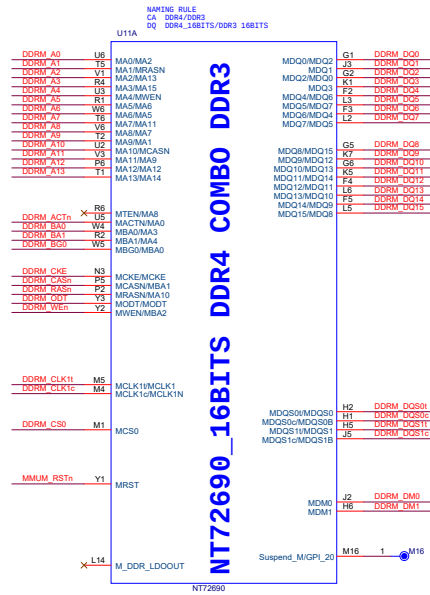




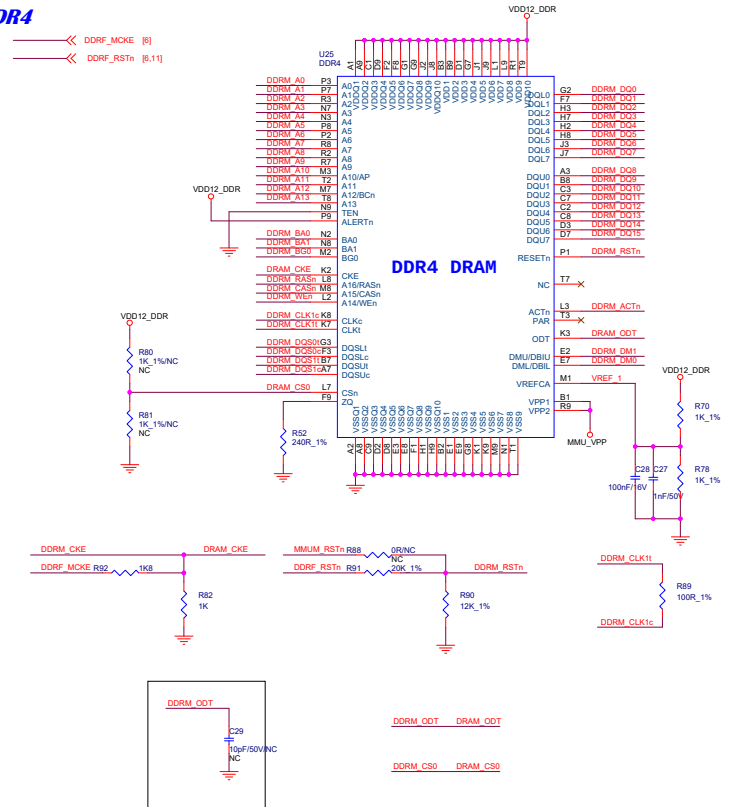
DDR_S



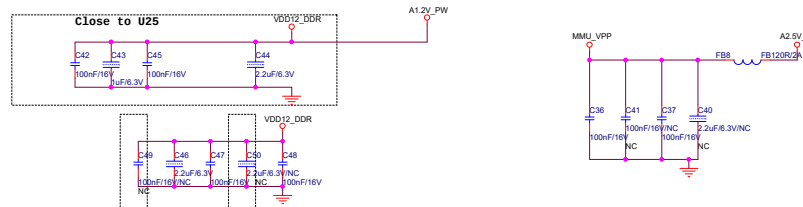
DDR_M



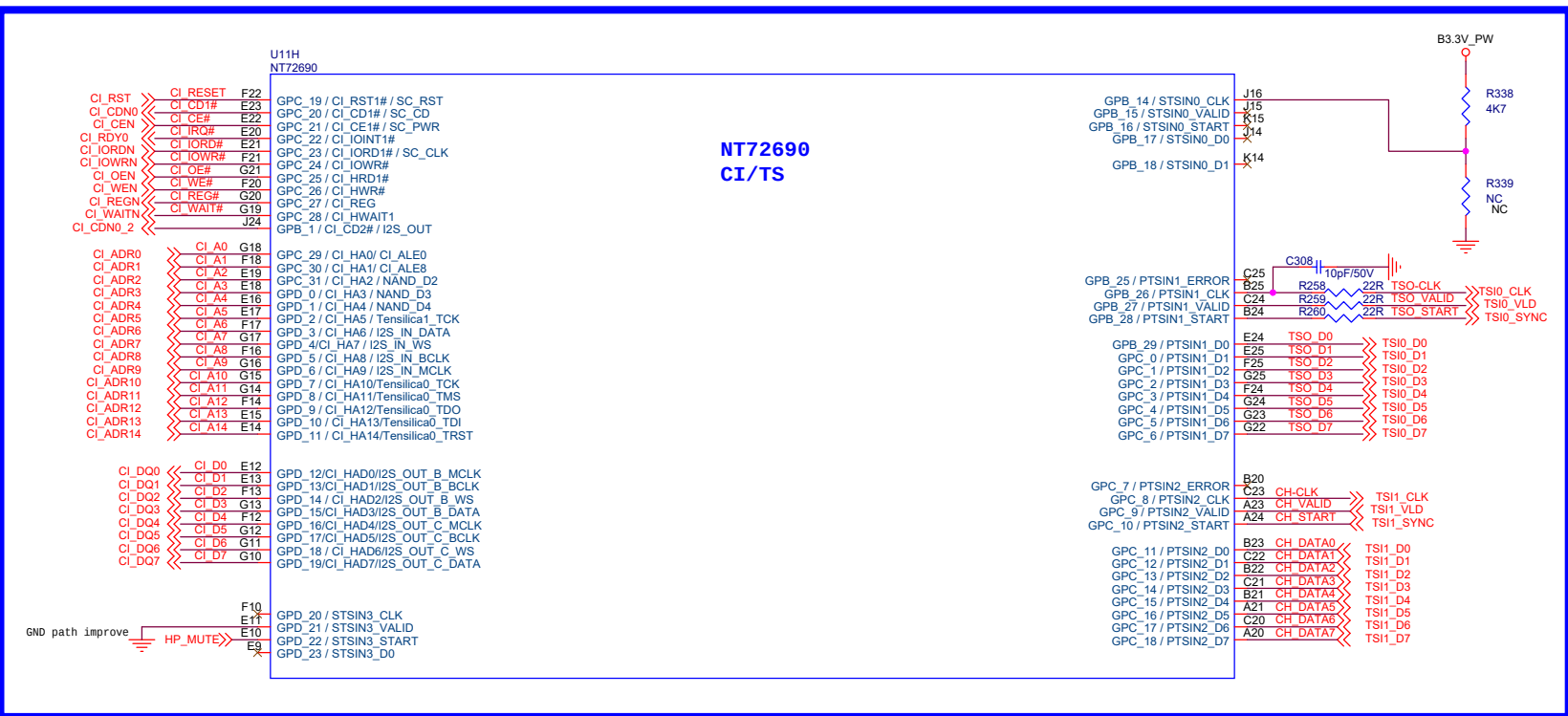
DDR4



DDR4_POWER



Title		Rev
Doc Number	06.DDR	V10
Date:	Thursday, May 23, 2024	Sheet 8 of 17



CPU Side:

BS0_Bypass CPU MaskROM

0 : Using CPU MaskROM
1 : Bypass CPU MaskROM

eMMC:

BS13_eMMC bus width

BS13 =
0: EMMC Bus width is 8 bit
1: EMMC Bus width is 4 bit

BS15_eMMC ACK

0: Boot mode wait ACK
1: Boot mode do not wait ACK

BS18_eMMC clk_switch

0: 26M
1: 13M

STBC Side:

BS1_STBC Boot Strap Option

0: Boot from STBC
1: Boot from CPU, bypass STBC.

BS8_STBC watchdog

0: Default disable STBC watchdog
1: Default enable STBC watchdog

BS19_Internal boot strap for NF/eMMC type

0: NF/eMMC type internal boot strap enable
1: NF/eMMC type internal boot strap disable
(BS[7:6] = 00, BS8 is external; BS[17:16]=00,BS14=0, BS13,BS15,BS18 are external)

BS2_Bypass STBC MaskROM

When BS1=0,
0: Through STBC MaskROM
1: Bypass STBC MaskROM

BS10_SPI Flash scramble

0: Disable
1: Enable

BS11_Turnkey Security

0: Disable
1: Enable

BS9_Security boot

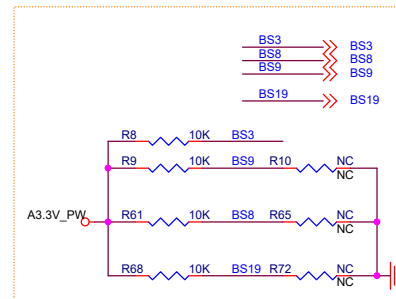
0: no security boot
1: security boot

BS20_NAND I/O

0: NAND I/O in STBC eMMC side (BS12 = 1)
1: NAND I/O in ARM CI side (BS12 = 1, BS[4:3] = 00, 11)
or STBC SPI side (BS12 = 1, BS[4:3] = 01, 10)

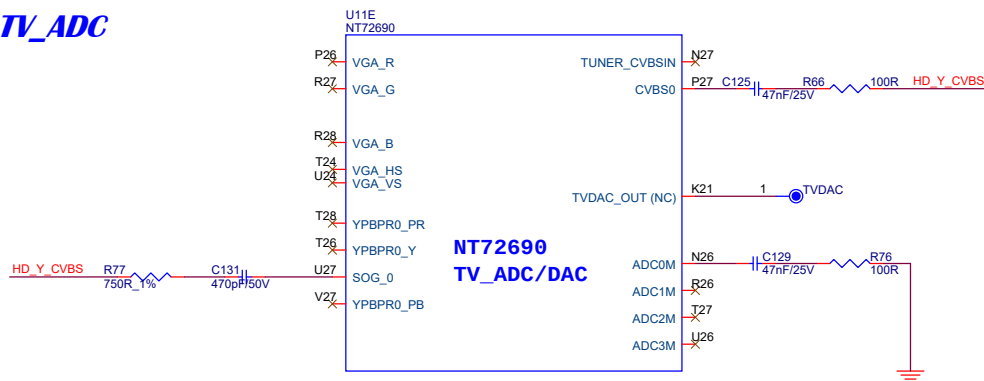
BS12=0 , BS3,BS4_Device

BS4, 3 =
00: STBC boot from SPI, CPU boot from eMMC
01: STBC & CPU both boot from eMMC
10: STBC & CPU both boot from SPI
11: Reserved (same 00)

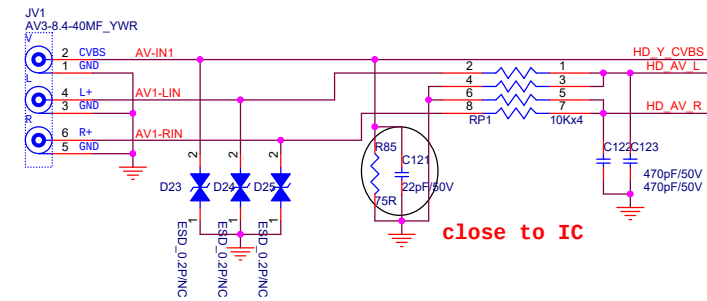


Size		Document Number		Title		Rev	
A3		07.CI/TS				V10	
Date:		Monday, May 20, 2024		Sheet		9 of 17	

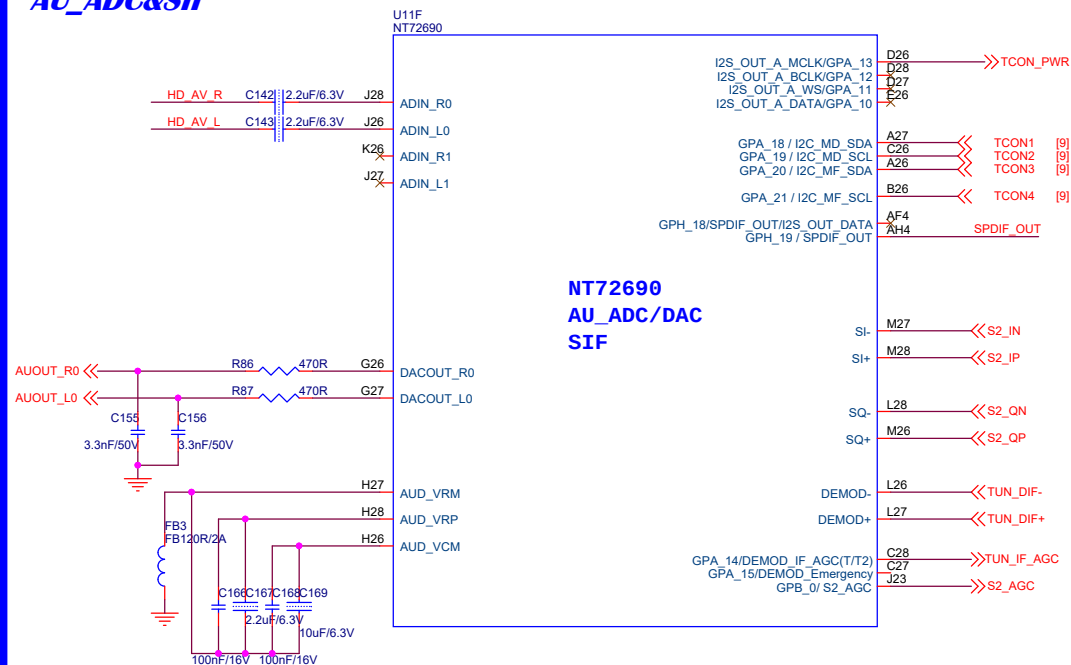
TV_ADC



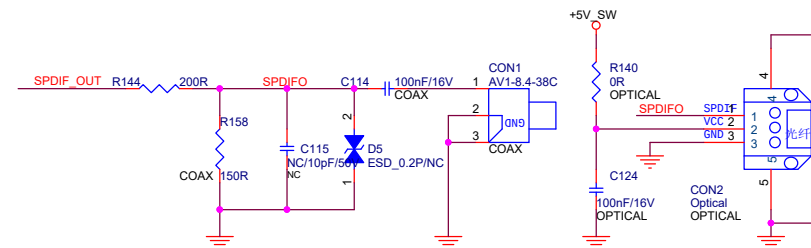
AV1_IN



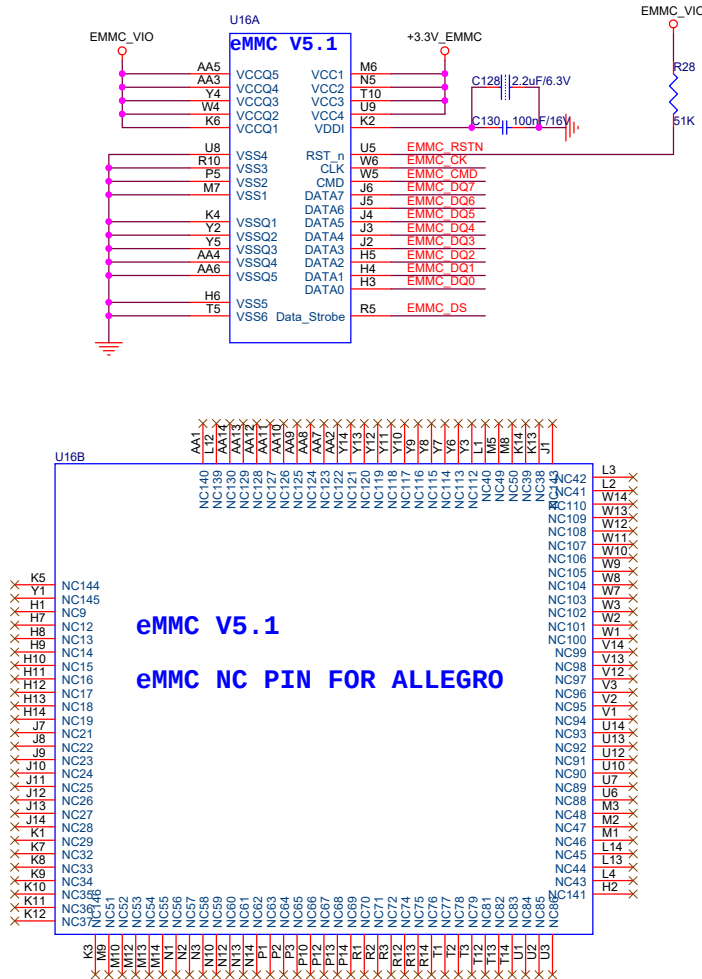
AU_ADC&SIF



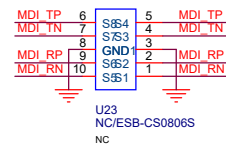
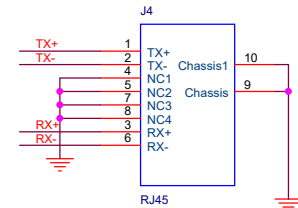
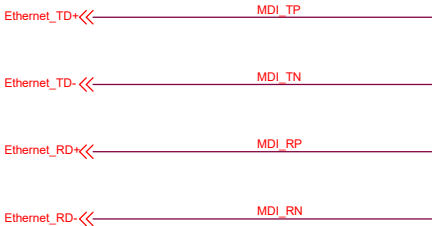
SPDIF OUT



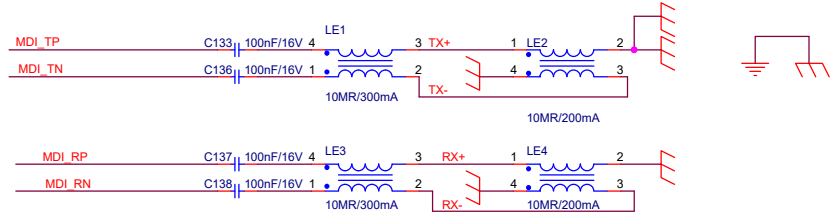
EMMC



Ethernet Connetor



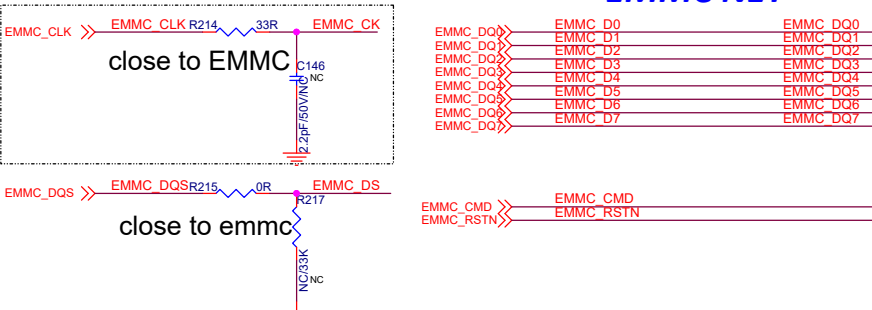
ENTHERNET 分立



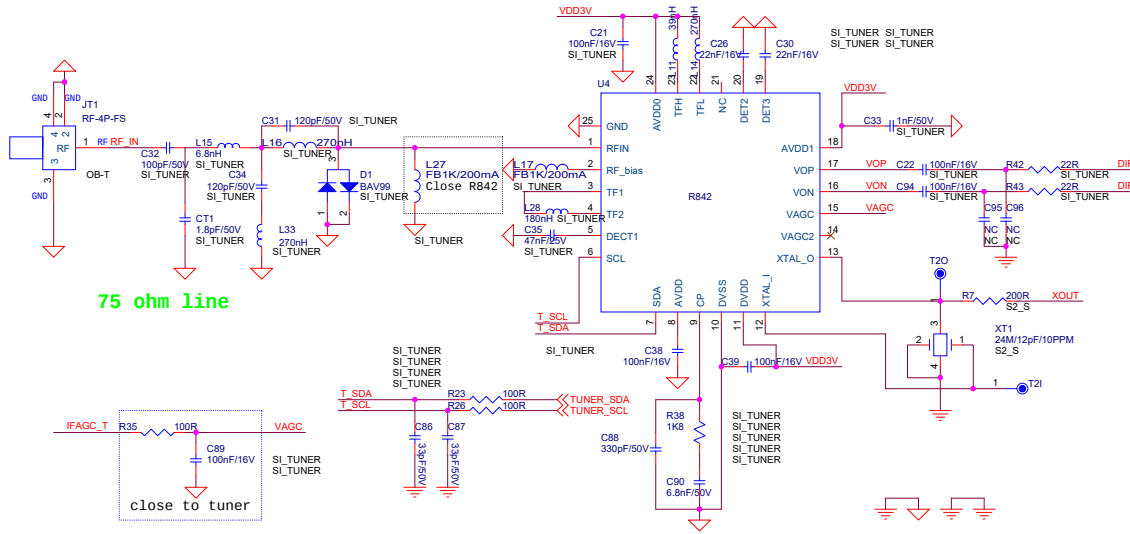
EMMC Power



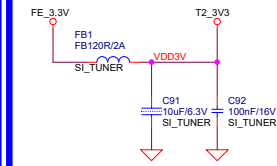
EMMC NET



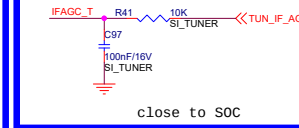
T/T2/C TUNER



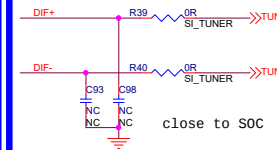
T2 Tuner Power



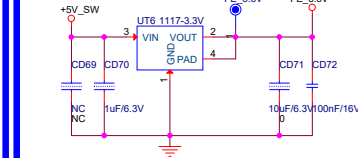
T2_AGC



T2_IF



Tuner Power

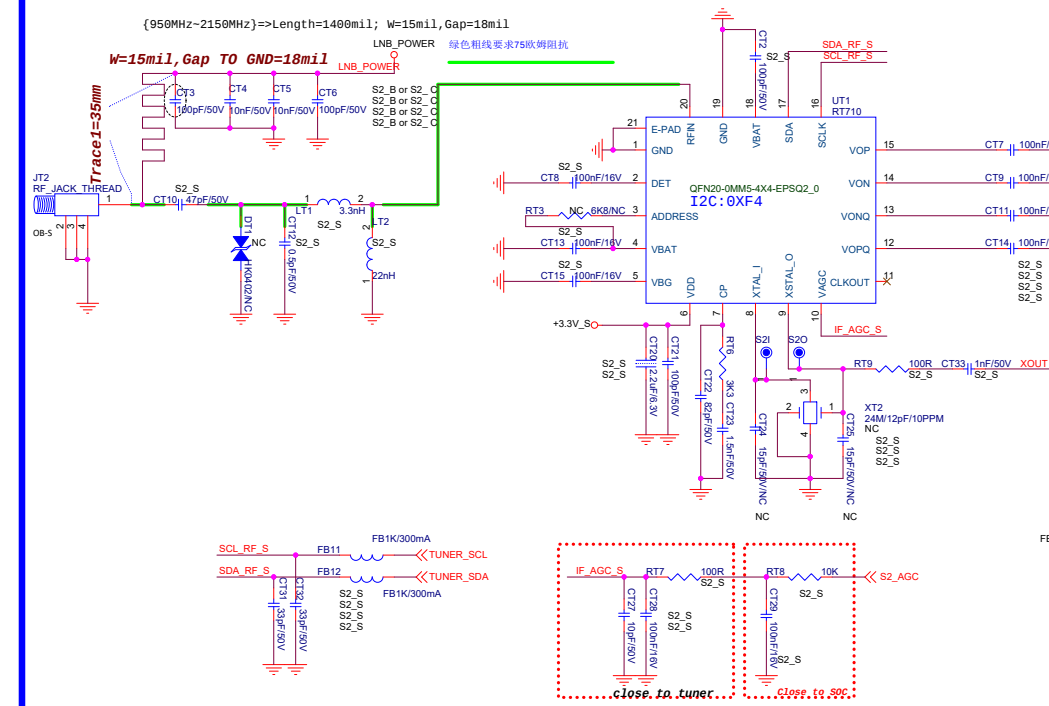


S2 TUNER

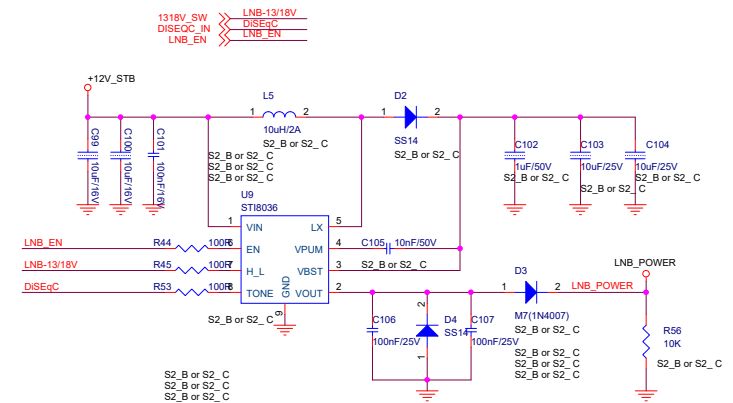
{950MHz~2150MHz}>=>Length=1400mil; W=15mil, Gap=18mil

W=15mil, Gap TO GND=18mil

LNB_POWER 绿色粗线要求75欧姆阻抗

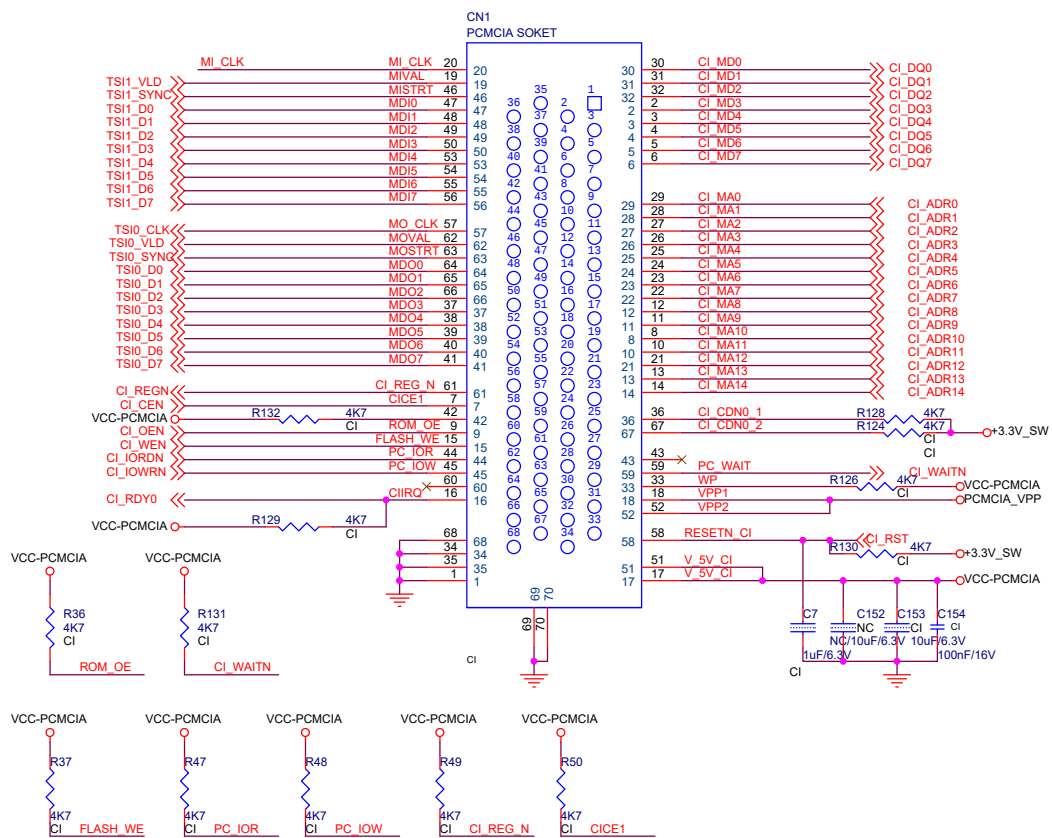


LNB POWER

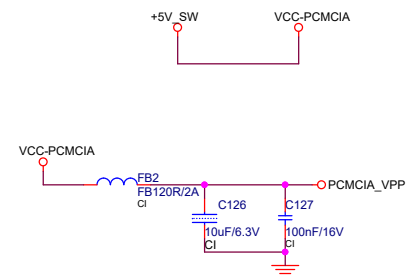
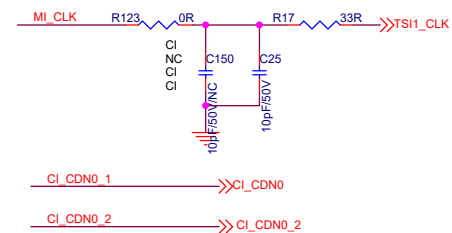


Title		11.T2&S2&LNB		Rev V10
Size	Document Number			
Custom				
Date:	Wednesday, May 29, 2024	Sheet	13	of 17

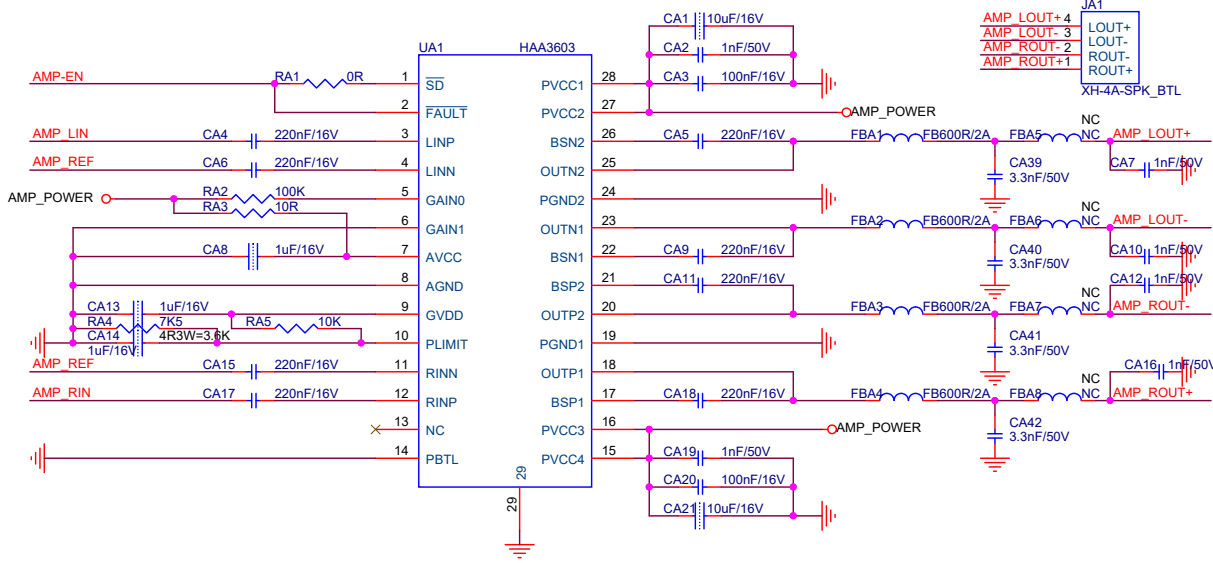
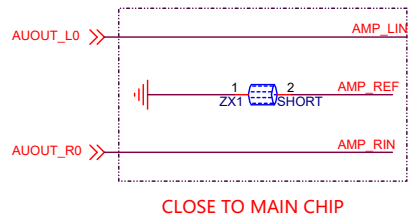
CI Socket



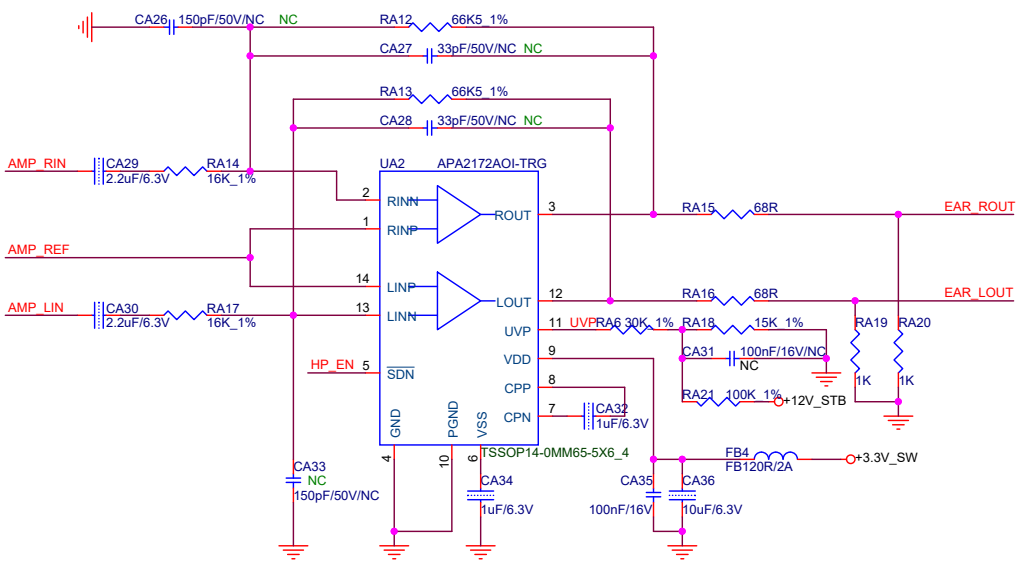
PCMCIA POWER

**CLK**

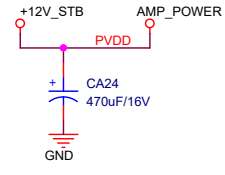
AMPLIFY



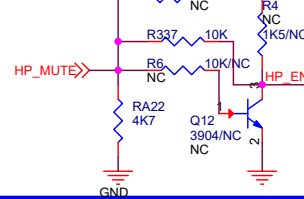
Headphone OP



POWER



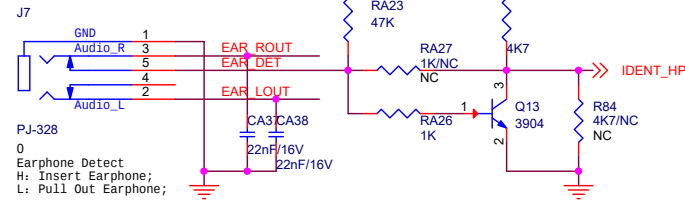
HP_MUTE



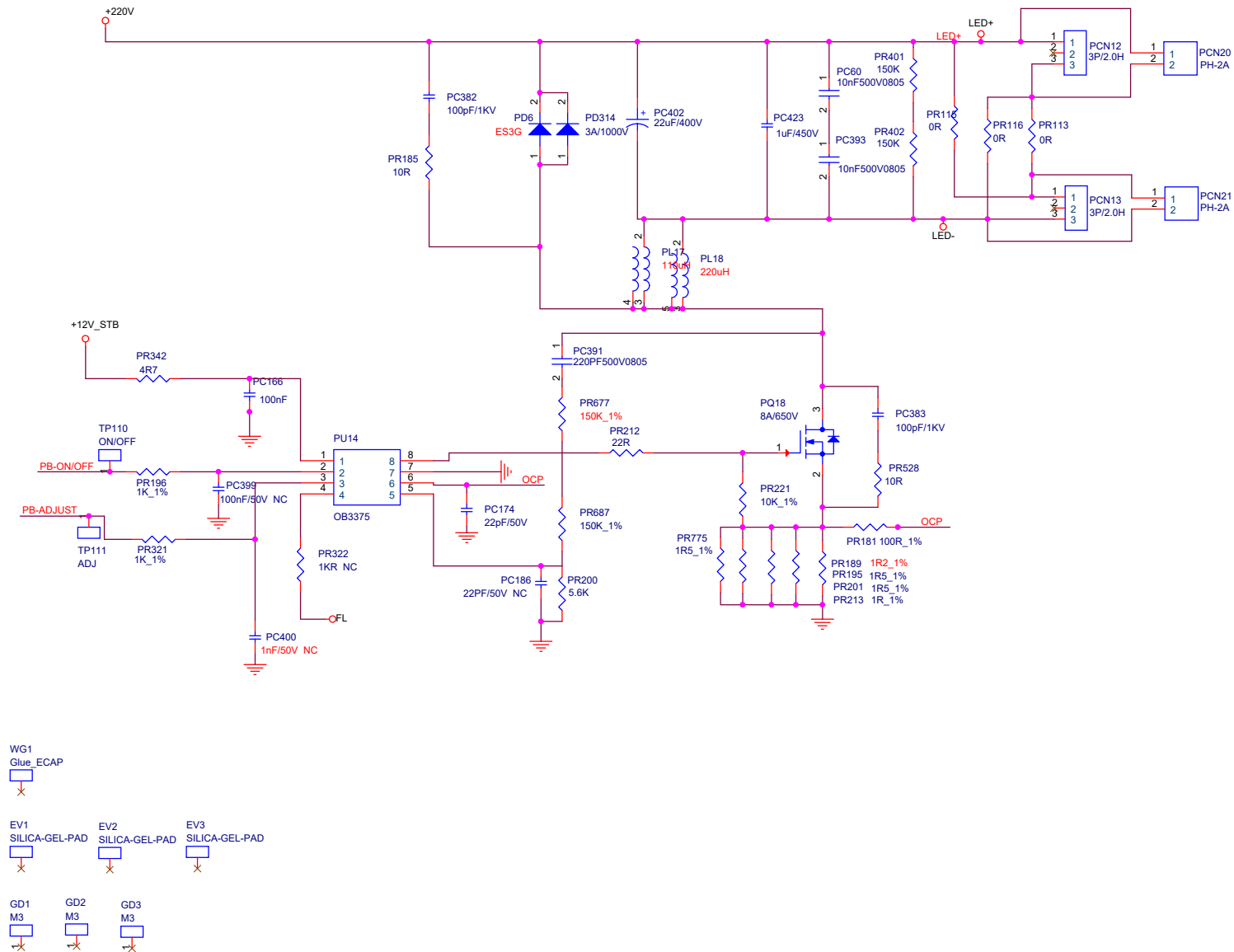
MUTE

AMP_MUTE
0 MUTE
1 NORMAL

EARPHONE



PB-ADJUST >> PB-ADJUST
PB-ON/OFF >> PB-ON/OFF



		Title	
		CV72690_D55	
Size	Document Number	Rev	
A3		10	
Date:		Sheet	
Friday, May 24, 2024		15 of 15	