

A close-up photograph of a computer motherboard. A central CPU is visible with its gold pins. To the left, two RAM modules are installed in their slots. Various electronic components like capacitors and integrated circuits are visible on the green PCB. Labels like 'U3', 'C108', 'C107', 'C113', 'C112', and 'U5' are printed on the board. The text 'MB281V SERVICE MANUAL' is overlaid on the right side of the image.

MB281V SERVICE MANUAL

Table of Contents

1. INTRODUCTION	3
A. GENERAL BLOCK DIAGRAM.....	4
B. PLACEMENT OF BLOCKS.....	5
2. T/T2/C/A Tuner (U12).....	6
3. S/S2 TUNER (U18).....	8
4. AUDIO AMPLIFIER STAGES.....	11
A. MAIN AMPLIFIER (U9) (10-W).....	11
5. POWER STAGE.....	14
A. PJS6415A (Q8).....	15
B. FDN336P (Q31)	17
C. DMG6402LDM (Q2)	18
D. TPS563201 (U1, U2)	19
E. JW5361M (U6)	21
F. MP1470HGJ (U16).....	23
G. APL5910 (U7)	24
6. MICROCONTROLLER	27
NOVATEK NT72564 (U19)	27
7. 4 GB EMMC.....	33
SAMSUNG EMMC 4GB KLM4G1FETE-B041 (U138)	33
8. USB INTERFACE.....	34
A. USB POWER SWITCH TPS25221 (U20)	35
9. CI INTERFACE.....	36
10. SOFTWARE UPDATE	36
MAIN SOFTWARE UPDATE.....	36
11. TROUBLESHOOTING.....	36
A. NO BACKLIGHT PROBLEM	36
B. CI MODULE PROBLEM.....	39
C. IR PROBLEM	40
D. USB PROBLEMS.....	41
E. NO SOUND PROBLEM	41
F. STANDBY ON/OFF PROBLEM	43
G. NO SIGNAL PROBLEM	43
12. SERVICE MENU SETTINGS	44

IMPORTANT

Before removing the rear cover from the TV for servicing, make sure that no cables are fixated to the cover. Release the cables from their clamps and disconnect (if any). Failure to do so may damage the wires and/or other components of the TV.

1. INTRODUCTION

17MB281 main board is driven by Novatek SOC. This IC is a single chip iDTV solution that supports channel decoding, MPEG decoding, and media-center functionality enabled by a high-performance AV CODEC and CPU.

This board can be driven just 50Hz HD and FHD panels.

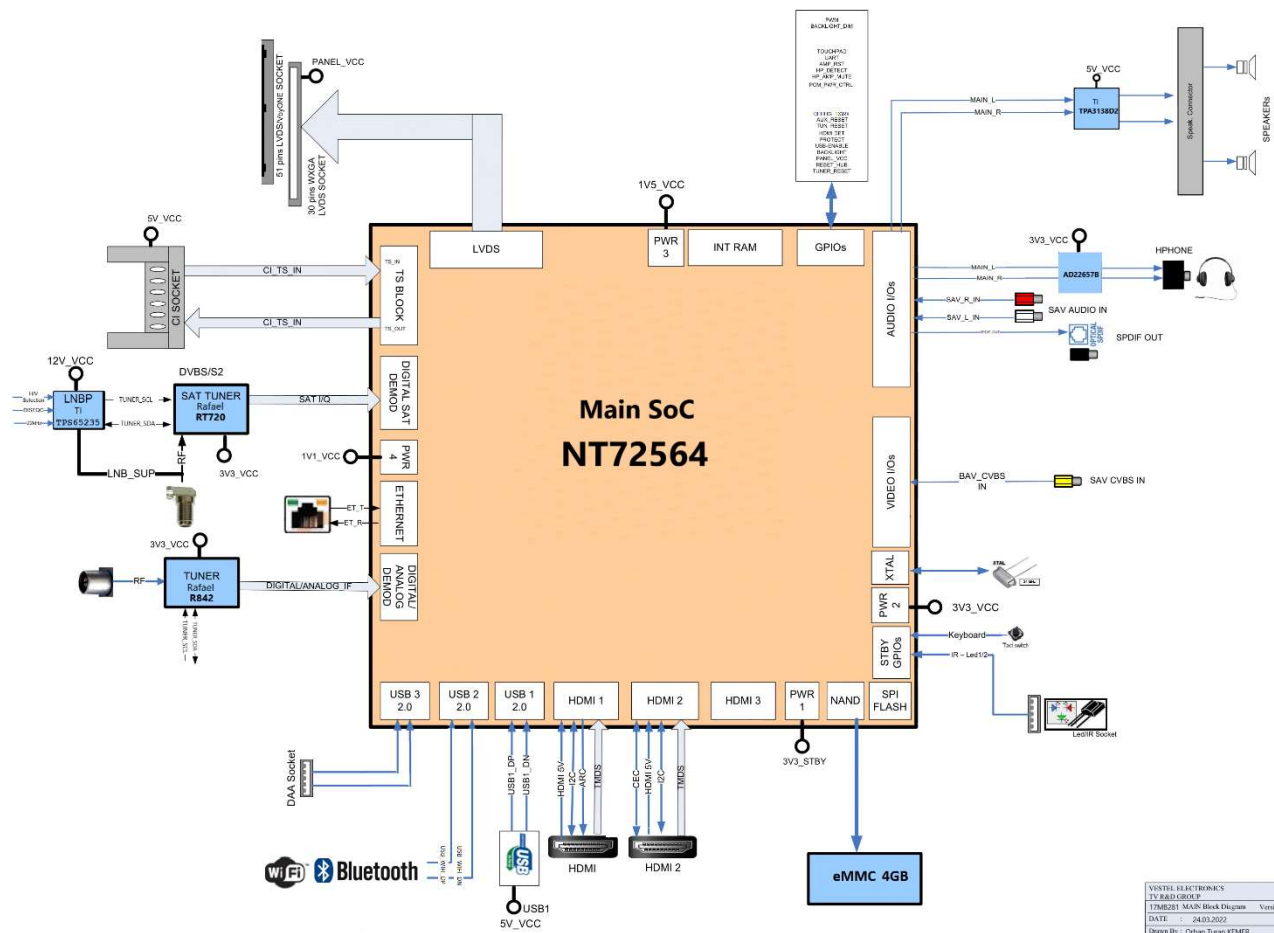
Key features include:

- Combo Front-End Demodulator
- A multi standart A/V format decoder
- Home theatre sound processor
- Fifth generation color engine
- Rich internet connectivity and completed digital home network solution
- Multi-purpose CPU for OS and multimedia
- Peripheral and power management
- Embedded DRAM

Supported peripherals are:

- 1 RF input VHF I, VHF III, UHF
- 1 Satellite input
- 1 Side AV (CVBS, R/L_Audio)
- 1xBack HDMI 1x Side HDMI input (with ARC option from 2nd input)
- 1 Common interface (Common)
- 1 Coax S/PDIF output
- 1 Headphone (Common)
- 1 USB (1X Side Common) and 1x internal USB for Wifi/Bluetooth
- 1 Ethernet-RJ45
- 1 Tact Switch

A. GENERAL BLOCK DIAGRAM



B. PLACEMENT OF BLOCKS

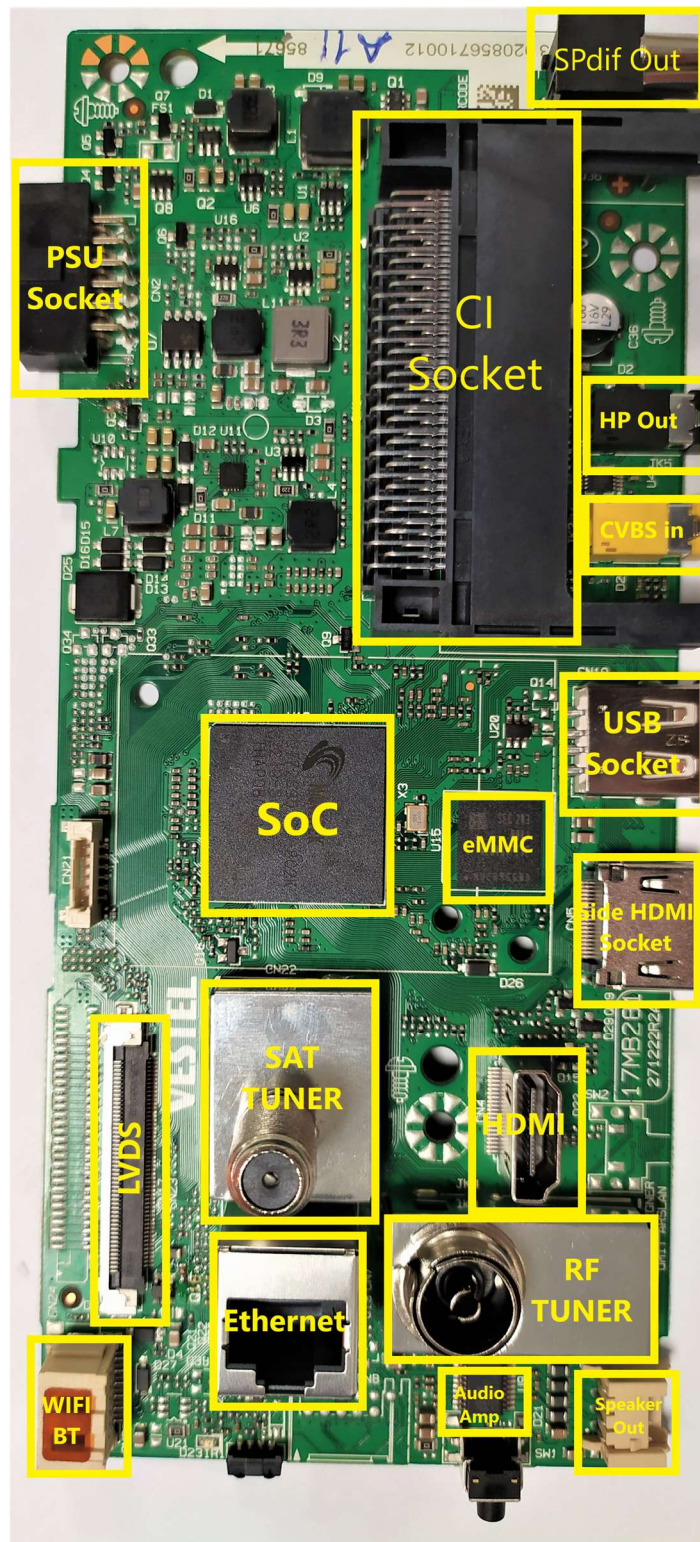


Figure 1: Placement of blocks

2. T/T2/C/A TUNER (U12)

Description

RT720 is a low-cost, direct-conversion tuner. Using for satellite signal receiving applications. It supports Digital Video Broadcast (DVB-S/S2) and further ABS-S or DVB-S2X applications.

RT720 directly converts the satellite signals from the LNB to baseband using a broadband I/Q down-converter. The operating frequency range extends from 250MHz to 2300MHz. The device includes an ultra low noise variable-gain LNA and a RF variable-gain amplifier, which is auto-controlled by integrated smart power detector and realize wide-dynamic range at the same time. The baseband low pass filters with variable cutoff frequency control support IF channel BW from 4MHz to 40MHz. The gain of baseband variable-gain amplifiers is controlled by VAGC pin to provide optimize ADC input power at demodulator.

RT720 has monolithic PLL architecture and integrated LDO; making the system achieves compact design with low BOM cost, and supplies single power pin to increase noise tolerance. RT720 is perfectly compliant with a small package, 20-pin QFN.

Features:

- Worldwide satellite standards supported
 - ISDB-S
 - DVB-S/S2
 - DVB-S2X
 - ABS-S
- Support all satellite system 250MHz to 2300MHz Frequency Range 42-1002 MHz frequency range
- Fully integrated PLL with monolithic VCO
- Integrated Ultra low noise LNA: NF = 2.7dB
- High Dynamic Range Input
- Integrated Variable BW low-pass filters, support 4MHz to 40MHz
- Single voltage +3.3V supply
- Address Application
- Supported 16MHz, 24MHz and 27MHz crystal with CL=16pF, ESR ≤ 30ohm.(please reference application note)
- High RF Input ESD protection technique.
- 4 differential IQ out & 2 single IQ out.
- Two AGC control mode- positive & negative, controlled by SW
- RF & IF RSSI

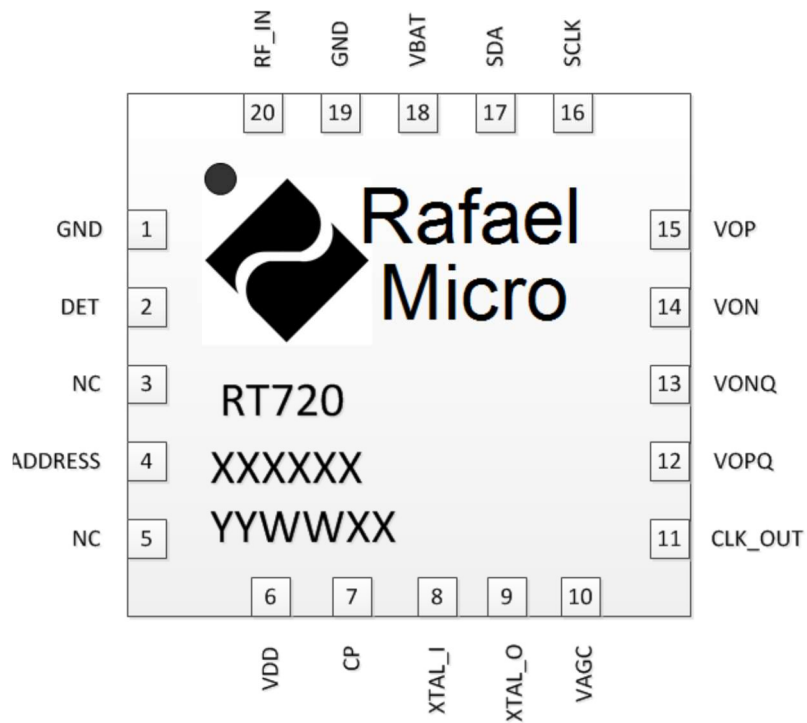


Figure 2: RT720 Pin description

Pin Number	Pin Name	I/O	Description
1	GND	S	GND
2	DET	-	RFAGC decoupling
3	NC	-	NC
4	Address	-	Address
5	NC	-	NC
6	VDD	S	3V3 LDO Input
7	CP	-	PLL Charge Pump Output (Off-chip Loop Filter needed)
8	XTAL_I	I	Crystal Input
9	XTAL_O	I	Crystal Output
10	VAGC	I	Voltage Gain Control Input
11	CLK_OUT	O	Clock Output for demodulator (Frequency = Crystal Frequency)
12	VOPQ	O	Quadrature Baseband Differential Output.
13	VONQ	O	Quadrature Baseband Differential Output.
14	VON	O	In-Phase Baseband Differential Output.
15	VOP	O	In-Phase Baseband Differential Output.
16	SCLK	I	I ² C Clock(Built-in the pull high resistance)
17	SDA	I/O	I ² C Data(Built-in the pull high resistance)
18	VBAT	S	Internal 3V decouple
19	GND	-	GND
20	RF_IN	I	RF input. (250MHz ~ 2300MHz)

Table 1: RT720 Pin function

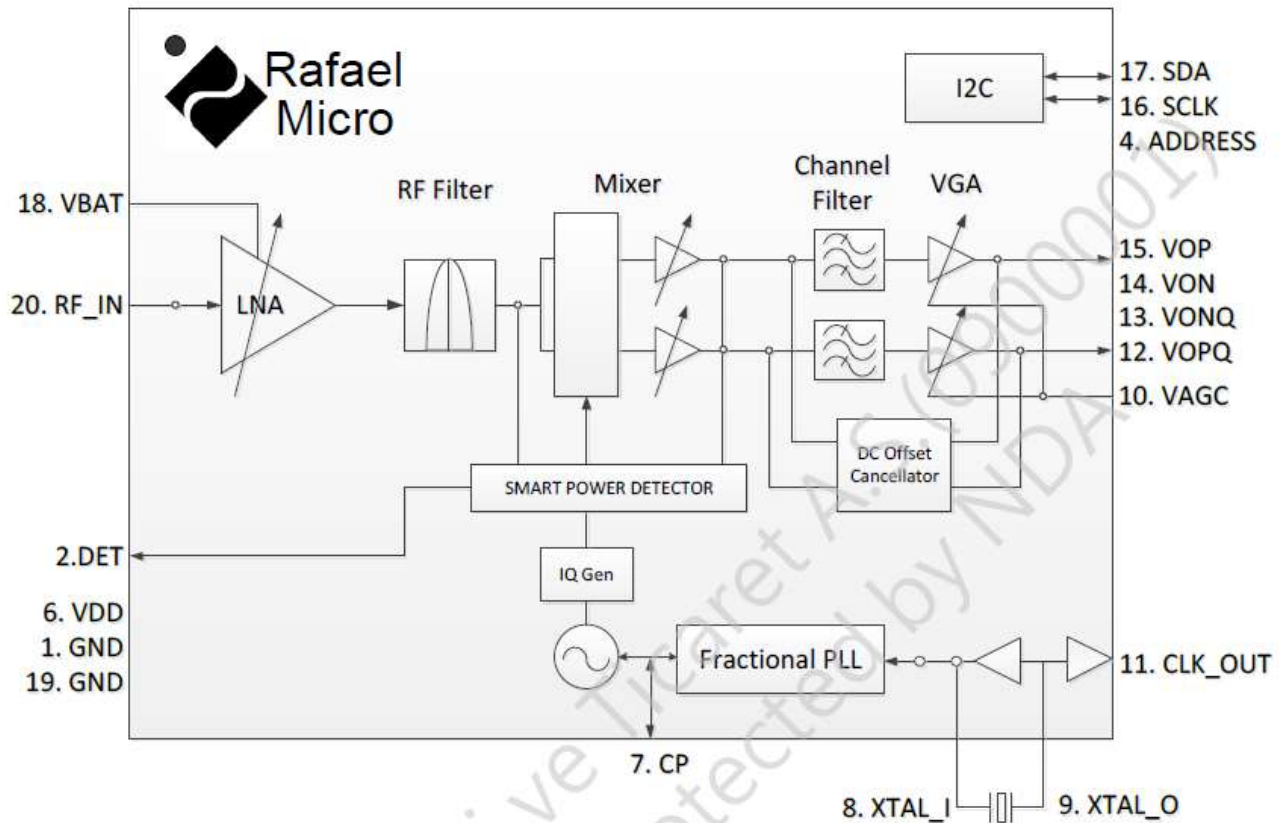


Figure 3: Block Diagram of RT720

3. S/S2 TUNER (U18)

Description

The R842 hybrid TV tuner utilizes state-of-the-art architecture to achieve high linearity with lowest power consumption. It offers unmatched RF performance for all analog and digital broadcast television standards including PAL, NTSC, SECAM, DVB-T/T2/C, J.83B, ATSC1.0, ATSC3.0, DTMB and ISDB-T/C. With innovative AccuTune™ and TrueRF™ mechanisms, the R842 provides superior performance in sensitivity, linearity, adjacent channel immunity and image rejection. A smart tracking filter and power detector adapt to various scenarios of input channels & power levels to optimize the spurious free dynamic range without any need for an external RF balun, LNA or SAW filter.

R842 is a highly integrated silicon tuner that builds in low noise amplifier (LNA), mixer, fractional PLL, VGA, voltage regulator and tracking filter, eliminating the need for external SAW filters, LNA and RF balun. High performance LNA, and small package enable R842 the perfect solution for both cost and performance sensitive applications.

With proprietary GreenRF techniques, R842 achieves both high performance and the lowest power consumption which perfectly compliant with the worldwide trend. R842 comes in a small and thin QFN RoHS compliant package.

Features

- Worldwide hybrid TV tuner
 - Analog: PAL, NTSC, SECAM
 - Digital: DVB-T/T2/C, ISDB-T/C, DTMB, ATSC1.0, ATSC3.0, J.83B
- Compliant with worldwide specifications
 - NorDig, D-BOOK, C-BOOK, ARIB, EN55020, Open Cable™
- All system channel support
 - 42MHz to 1002MHz
- Lowest BOM cost
 - No need for SAW filter, external LNA and RF balun
- Low power consumption
- Best-in-class adjacent channel immunity in real-world environments to outperform in all situations
- Standard I2C control interface
- 4x4 24-pin QFN E-pad package
- Environmental compliance: Halogen-free / RoHS 2.0 / Reach Annex 14 & 17

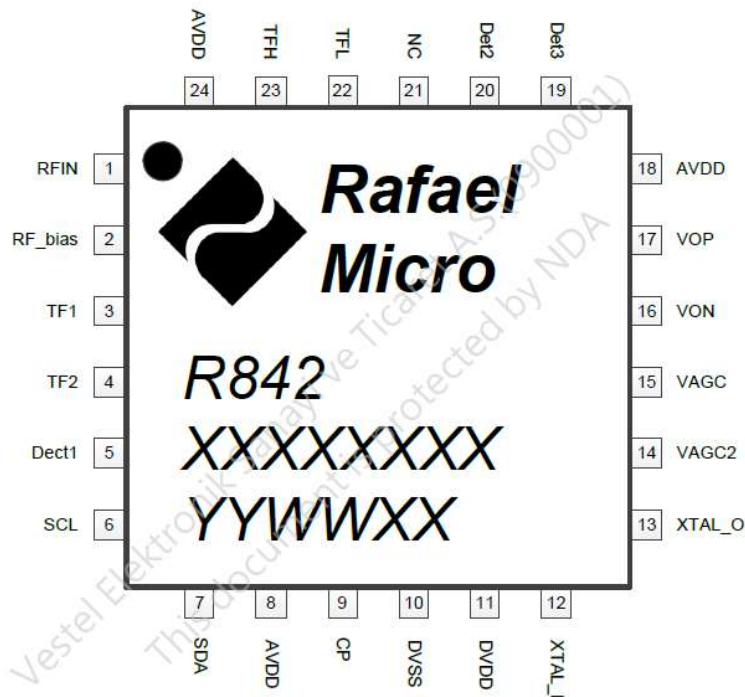


Figure 4: Pin Configuration of R842

Block Diagram

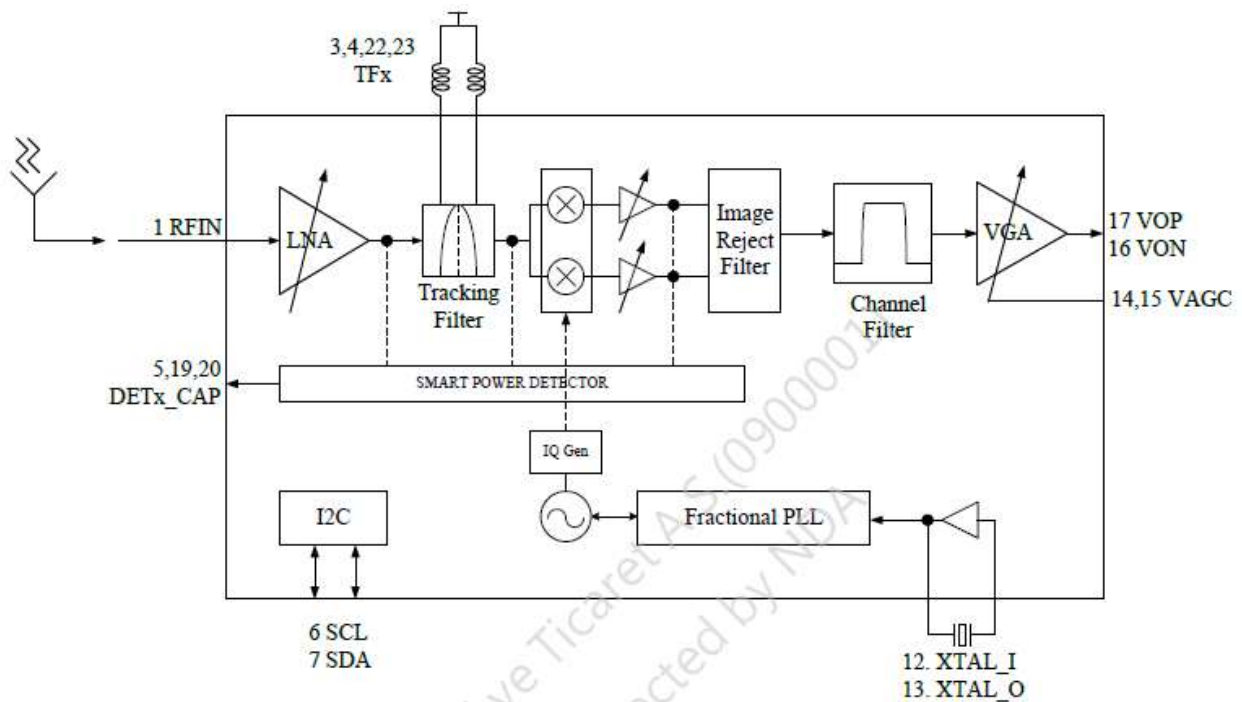


Figure 5: Block diagram of R842

Pin Number	Symbol	I/O	Description
1	RFIN	I	RF input
2	RF_bias	-	RF circuit bias
5,19,20	Det1,2,3	-	Power detector decoupling capacitor
3,4,22,23	TF1,2,H,L	-	Tracking filter pins
6	SCL	I	I ² C Clock
7	SDA	I/O	I ² C Data
8	AVDD	S	AVDD for PLL
9	CP	-	PLL Charge Pump decouple
10	DVSS	S	Digital Ground
11	DVDD	S	Digital 3.3V Supply
12	XTAL_I	I	Crystal Driver
13	XTAL_O	I	Crystal Driver
14,15	VAGC	I	Voltage Gain Control Input
16,17	VOP, VON	O	Differential IF Output
18	AVDD	S	Analog 3.3V Supply
21	NC	-	Not used (no connection)
24	AVDD	S	RF 3.3V Supply

Table 2: Pin function of R842

4. AUDIO AMPLIFIER STAGES

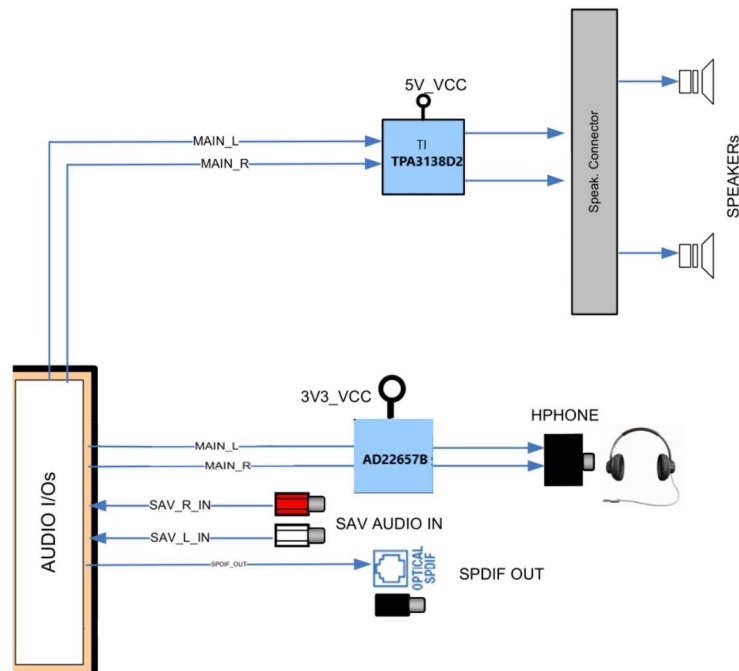


Figure 6: The block diagram of the audio part

A. MAIN AMPLIFIER (U9) (10-W)

Description

The TPA3138D2 is a 10-W/ch, high-efficiency, lowidle-current Class-D stereo audio amplifier. It can drive stereo speakers with a load as low as 3.2- Ω . In the 1SPW mode, it consumes a low idle current of only 21-mA (12-V) and can operate down to 3.5-V, allowing for longer audio play and improved thermal performance in bluetooth speakers, battery-powered appliances and other power-sensitive applications. Advanced EMI Suppression with Spread Spectrum Control enables the use of inexpensive ferrite bead filters while meeting EMC requirements for system cost reduction. To further simplify the design, the TPA3138D2 integrates essential protection features including undervoltage, overvoltage, power limit, short circuit, overtemperature, as well as DC speaker protection. All of these protections come with automatic recovery. Customers can leverage every TPA3138D2 feature in existing designs as it is fully pin-to-pin compatible to TI's TPA3110D2, TPA3136D2 and TPA3136AD2.

Features

- Wide Supply Range 3.5-V to 14.4-V
 - 2×10 W into 6- Ω , 1% THD+N, 12-V Supply
 - 1×18.5 W into 4- Ω , 10% THD+N, 12-V Supply
 - THD+N : 0.04% at 1 W, 1 kHz input, 6- Ω
- Longer Battery Life for Portable Applications:
 - 20-mA (12-V) Idle Current in 1SPW Mode

- >90% Class-D Efficiency
- Reduced Solution Size and Cost:
 - Inductor-Free Operation
 - EN55013 and EN55022 EMC Compliant When No Inductors are Used
 - No External Heatsink Required
- Flexible Audio Solution:
 - Single-ended or Differential Analog Inputs
 - Selectable Gain: 20 dB and 26 dB
 - Pop and Click-Free Startup
- Integrated Protections and Auto Recovery:
 - Pin-to-pin, Pin-to-Ground, and Pin-to-Power Short Circuit Protection
 - Thermal Protection, Undervoltage Protection, and Overvoltage Protection
 - Power Limiter and DC Speaker Protection
- Pin-to-Pin Compatible with TPA3110D2, TPA3136D2 and TPA3136AD2

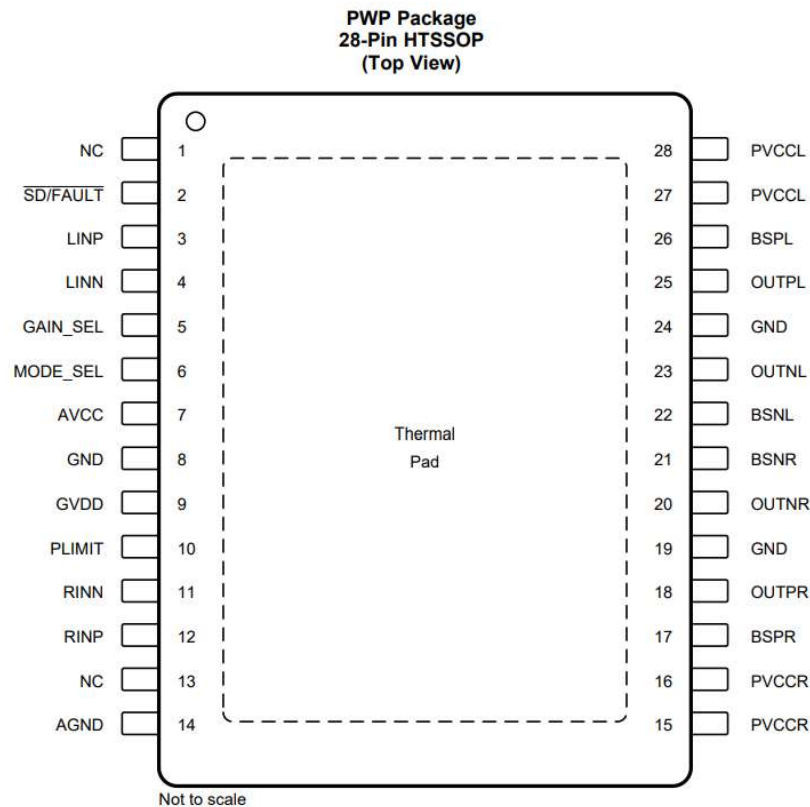


Figure 7: Pin description of amplifier

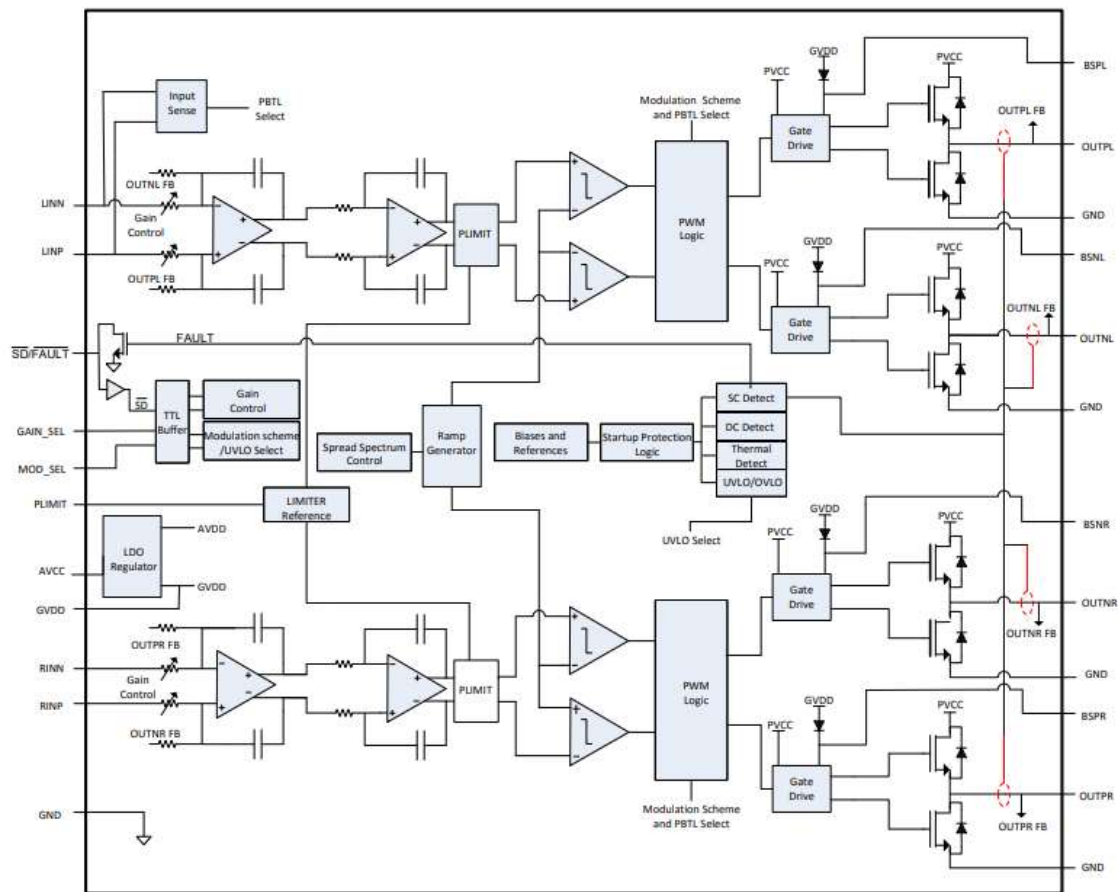


Figure 8: Functional Block Diagram of TPA3138D2

		MIN	MAX	UNIT
Supply voltage	AVCC to GND, PVCC to GND	−0.3	20	V
Input current	To any pin except supply pins	10		mA
Interface pin voltage	$\overline{\text{SD/FAULT}}$ to GND ⁽²⁾ , GAIN_SEL, MODE_SEL	−0.3	AVCC + 0.3	V
		10		V/ms
	PLIMIT	−0.3	GVDD + 0.3	V
	RINN, RINP, LINN, LINP	−0.3	5.5	V
Minimum load resistance, R _L	BTL, (10 V < PVCC < 14.4 V)	4.8		Ω
	BTL, (3.5 V < PVCC < 10 V)	3.2		
	PBTL, (10 V < PVCC < 14.4 V)	2.4		
	PBTL, (3.5 V < PVCC < 10 V)	1.6		
Continuous total power dissipation		See the Thermal Information Table		
Operating Junction Temperature range		−25	150	°C
Storage temperature range, T _{stg}		−40	125	°C

Table 3: Absolute Maximum Ratings of TPA3138D2

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V _{CC}	Supply voltage	PVCC, AVCC	3.5	14.4	V
V _{IH}	High-level input voltage	$\overline{SD/FAULT}^{(1)}$, GAIN_SEL, MODE_SEL	2	AVCC	V
V _{IL}	Low-level input voltage	$\overline{SD/FAULT}$, GAIN_SEL, MODE_SEL ⁽²⁾		0.8	V
V _{OL}	Low-level output voltage	$\overline{SD/FAULT}$, R _{PULL-UP} = 100 k Ω , PVCC = 14.4 V		0.8	V
I _{IH}	High-level input current	$\overline{SD/FAULT}$, GAIN_SEL, MODE_SEL, V _I = 2 V, AVCC = 12 V		50	μ A
I _{IL}	Low-level input current	$\overline{SD/FAULT}$, GAIN_SEL, MODE_SEL, V _I = 0.8 V, AVCC = 12 V		5	μ A
T _A	Operating free-air temperature ⁽³⁾		-10	85	°C
T _J	Operating junction temperature ⁽³⁾		-10	150	°C

Table 4: Recommended Operating Conditions

5. POWER STAGE

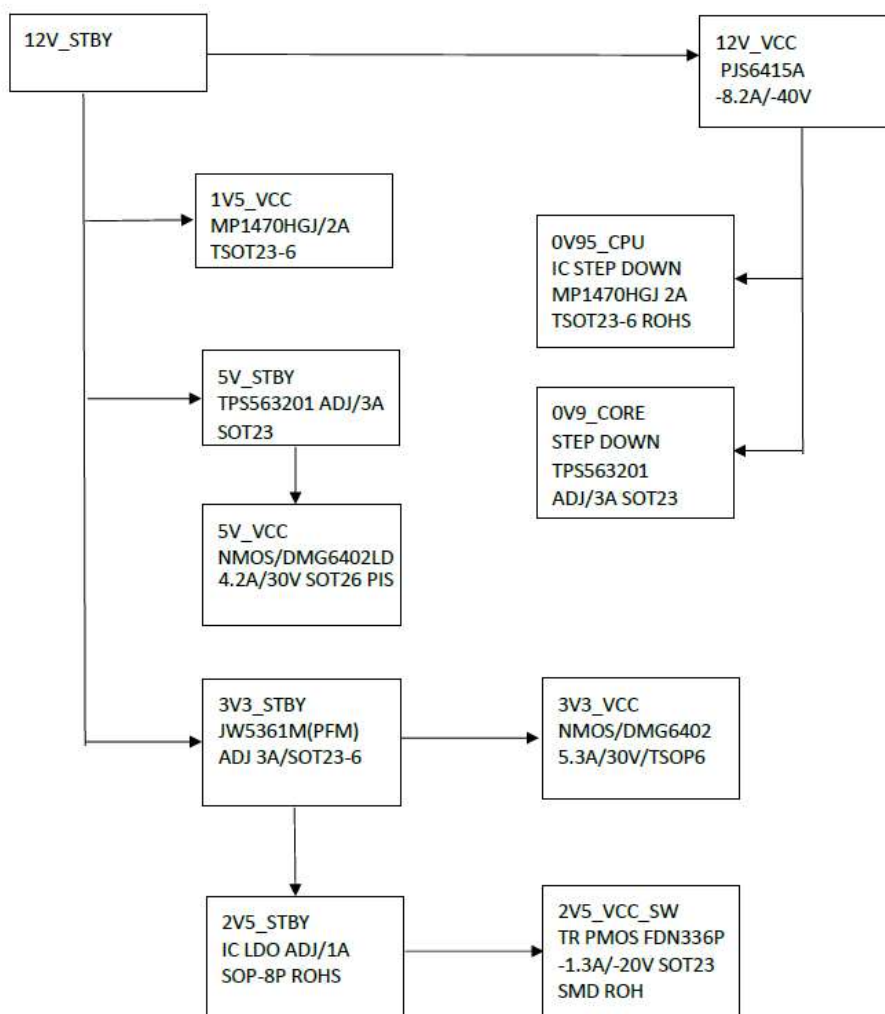


Figure 9: Power Block Diagram

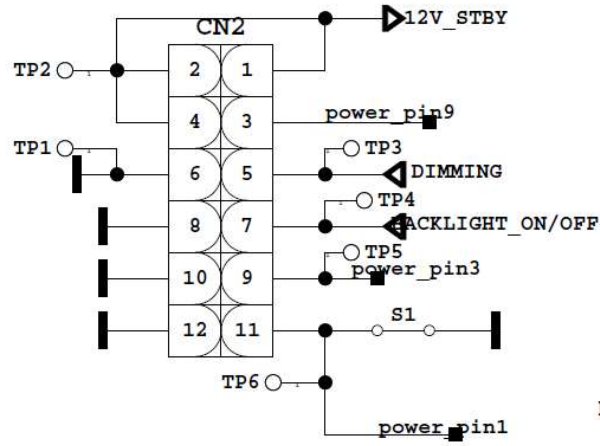


Figure 10: Power Socket and Power Options

Power socket is used for taking voltage which is 12V_STBY. These voltages are produced in power card. Also socket is used for giving dimming, backlight and standby signals with power card. Power socket pinning is shown in above figure.

12V_STBY is converted several different voltages on the mainboard which are shown in below figure.

List of the components:

- PMOS(Q8) → PJS6415A
- PMOS(Q31) → FDN336P
- NMOS(Q2) → DMG6402LDM
- DC-DC-1(U1) → TPS563201
- DC-DC-2(U6) → JW5361M(PFM)-3A
- DC-DC-3(U16) → MP1470HGX-2A
- DC-DC-4(U2) → TPS563201
- DC-DC-5(U3) → MP1470HGX
- LDO(U7) → ADJ/1A SOP-8P

A. PJS6415A (Q8)

Features

- VDS (V) = -20V
- RDS(ON) < 46mΩ (VGS = -4.5V ID = -5.2A)
- RDS(ON) < 56mΩ (VGS = -2.5V ID = -3.0A)
- RDS(ON) < 88mΩ (VGS = -1.8V ID = -1.5A)

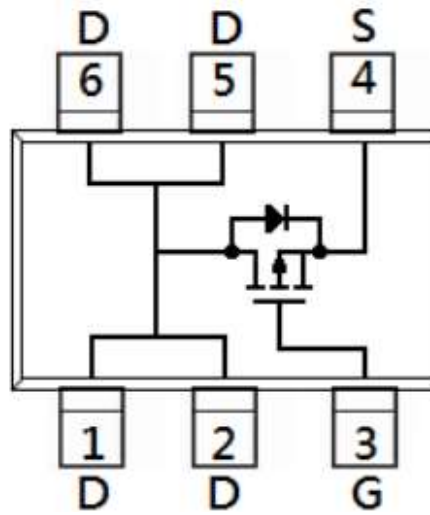


Figure 11: Pin description

Electrical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-20	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.5	-0.74	-1.3	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=-4.5V, I_D=-5.2A$	-	38	46	mΩ
		$V_{GS}=-2.5V, I_D=-3.0A$	-	47	56	
		$V_{GS}=-1.8V, I_D=-1.5A$	-	68	88	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-16V, V_{GS}=0V$	-	-	-1	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 12V, V_{DS}=0V$	-	-	±100	nA
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=-10V, I_D=-5.2A,$ $V_{GS}=-4.5V$ (Note 1,2)	-	10	-	nC
Gate-Source Charge	Q_{gs}		-	1.7	-	
Gate-Drain Charge	Q_{gd}		-	2.4	-	
Input Capacitance	C_{iss}	$V_{DS}=-10V, V_{GS}=0V,$ $f=1.0MHz$	-	980	-	pF
Output Capacitance	C_{oss}		-	100	-	
Reverse Transfer Capacitance	C_{rss}		-	81	-	
Switching						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD}=-10V, I_D=-5.2A,$ $V_{GS}=-4.5V,$ $R_G=6\Omega$ (Note 1,2)	-	9.8	-	ns
Turn-On Rise Time	t_r		-	54	-	
Turn-Off Delay Time	$t_{d(off)}$		-	44	-	
Turn-Off Fall Time	t_f		-	31	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I_S	---	-	-	-2.0	A
Diode Forward Voltage	V_{SD}	$I_S=-1.0A, V_{GS}=0V$	-	-0.78	-1.2	V

Table 5: Electrical Characteristic

B. FDN336P (Q31)

Features

- -1.3 A , -20 V
 - ♦ $R_{DS(on)} = 0.20\text{ }\Omega$ $V_{GS} = -4.5\text{ V}$
 - ♦ $R_{DS(on)} = 0.27\text{ }\Omega$ $V_{GS} = -2.5\text{ V}$
- Low Gate Charge (3.6 nC Typical)
- High Performance Trench Technology for Extremely Low $R_{DS(ON)}$
- SUPERSOTTM –3 Provides Low $R_{DS(ON)}$ and 30% Higher Power
- Handling Capability than SOT23 in the Same Footprint

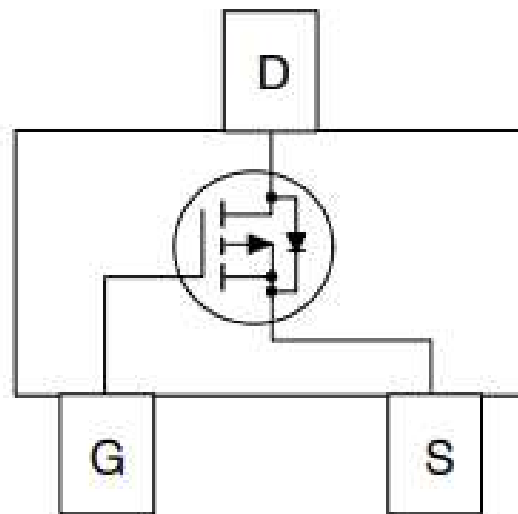


Figure 12: Pin description

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	250	$^{\circ}\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	75	$^{\circ}\text{C/W}$

ELECTRICAL CHARACTERISTICS $T_A = 25^{\circ}\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-20	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$, Referenced to 25°C	-	-16	-	mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V}$	-	-	-1	μA
		$V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V}, T_J = 55^\circ\text{C}$	-	-	-10	μA
I_{GSSF}	Gate-Body Leakage Forward	$V_{GS} = 8\text{ V}, V_{DS} = 0\text{ V}$	-	-	100	nA
I_{GSSR}	Gate-Body Leakage Reverse	$V_{GS} = -8\text{ V}, V_{DS} = 0\text{ V}$	-	-	-100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-0.4	-0.9	-1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$, Referenced to 25°C	-	3	-	mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -4.5\text{ V}, I_D = -1.3\text{ A}$	-	0.122	0.2	Ω
		$V_{GS} = -4.5\text{ V}, I_D = -1.3\text{ A}, T_J = 125^\circ\text{C}$	-	0.18	0.32	
		$V_{GS} = -2.5\text{ V}, I_D = -1.1\text{ A}$	-	0.19	0.27	
$I_{D(on)}$	On-State Drain Current	$V_{GS} = -4.5\text{ V}, V_{DS} = -5\text{ V}$	-5	-	-	A
g_{FS}	Forward Transconductance	$V_{DS} = -4.5\text{ V}, I_D = -2\text{ A}$	-	4	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	-	330	-	pF
C_{oss}	Output Capacitance		-	80	-	pF
C_{rss}	Reverse Transfer Capacitance		-	35	-	pF
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -5\text{ V}, I_D = -0.5\text{ A}, V_{GS} = -4.5\text{ V}, R_{GEN} = 6\text{ }\Omega$	-	7	15	ns
t_r	Turn-On Rise Time		-	12	22	ns
$t_{d(off)}$	Turn-Off Delay Time		-	16	26	ns
t_f	Turn-Off Fall Time		-	5	12	ns
Q_g	Total Gate Change	$V_{DS} = -10\text{ V}, I_D = -2\text{ A}, V_{GS} = -4.5\text{ V}$	-	3.6	5	nC
Q_{gs}	Gate-Source Change		-	0.8	-	nC
Q_{gd}	Gate-Drain Change		-	0.7	-	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		-	-	-0.42	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -0.42\text{ A}$ (Note 2)	-	-0.7	-1.2	V

Table 6: Electrical Characteristics & Maximum ratings

C. DMG6402LDM (Q2)

- Low $R_{DS(ON)}$
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- Lead Free By Design/RoHS Compliant (Note 1)
- Qualified to AEC-Q101 Standards for High Reliability
- "Green" Device (Note 2)

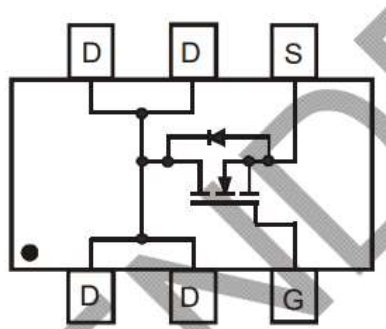


Figure 13: Pin Assignment

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 3)	P_D	1.12	W
Thermal Resistance, Junction to Ambient $T_A = 25^\circ\text{C}$ (Note 3)	$R_{\theta JA}$	111	$^\circ\text{C/W}$
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

Electrical Characteristics @ $T_A = 25^\circ\text{C}$ unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 5)						
Drain-Source Breakdown Voltage	BV_{DSS}	30	-	-	V	$V_{GS} = 0V, I_D = 250\mu A$
Zero Gate Voltage Drain Current $T_J = 25^\circ\text{C}$	I_{DSS}	-	-	1.0	μA	$V_{DS} = 30V, V_{GS} = 0V$
Gate-Source Leakage	I_{GSS}	-	-	± 100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
ON CHARACTERISTICS (Note 5)						
Gate Threshold Voltage	$V_{GS(th)}$	1.0	1.5	2.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
Static Drain-Source On-Resistance	$R_{DS(on)}$	-	22 32	27 40	m Ω	$V_{GS} = 10V, I_D = 7A$ $V_{GS} = 4.5V, I_D = 5.6A$
Forward Transfer Admittance	$ Y_{fs} $	-	10	-	S	$V_{DS} = 5V, I_D = 7A$
Diode Forward Voltage	V_{SD}	-	0.75	1.0	V	$V_{GS} = 0V, I_S = 1A$
DYNAMIC CHARACTERISTICS (Note 6)						
Input Capacitance	C_{iss}	-	404	-	pF	$V_{DS} = 15V, V_{GS} = 0V,$ $f = 1.0MHz$
Output Capacitance	C_{oss}	-	52	-	pF	
Reverse Transfer Capacitance	C_{rss}	-	45	-	pF	
Gate Resistance	R_g	-	1.51	-	Ω	$V_{DS} = 0V, V_{GS} = 0V, f = 1MHz$
Total Gate Charge	Q_g	-	9.2	-	nC	$V_{GS} = 10V, V_{DS} = 15V, I_D = 5.8A$
Gate-Source Charge	Q_{gs}	-	1.2	-	nC	
Gate-Drain Charge	Q_{gd}	-	1.8	-	nC	
Turn-On Delay Time	$t_{D(on)}$	-	3.41	-	ns	$V_{DD} = 15V, V_{GS} = 10V,$ $R_L = 2.6\Omega, R_G = 3\Omega$
Turn-On Rise Time	t_r	-	6.18	-	ns	
Turn-Off Delay Time	$t_{D(off)}$	-	13.92	-	ns	
Turn-Off Fall Time	t_f	-	2.84	-	ns	

Table 7: Thermal Characteristics & Electrical Characteristics

D. TPS563201 (U1, U2)

Features

- TPS563201 and TPS563208 3-A Converter Integrated 95-m Ω and 57-m Ω FETs.
- D-CAP2™ Mode Control with fast transient response
- Input Voltage Range: 4.5 V to 17 V
- Output Voltage Range: 0.76 V to 7 V
- Pulse-skip mode (TPS563201) or Continuous Current Mode (TPS563208)

- 580-kHz Switching Frequency
- Low Shutdown Current Less than 10 μ A
- 2% Feedback Voltage Accuracy (25 °C)
- Startup from Pre-Biased Output Voltage
- Cycle-by-Cycle Overcurrent Limit
- Hiccup-mode Overcurrent Protection
- Non-Latch UVP and TSD Protections
- Fixed Soft Start: 1.0 ms

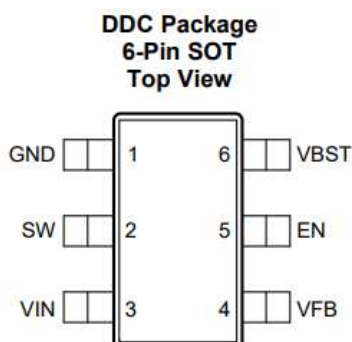


Figure 14: Pin Assignment

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	1	—	Ground pin Source terminal of low-side power NFET as well as the ground terminal for controller circuit. Connect sensitive VFB to this GND at a single point.
SW	2	O	Switch node connection between high-side NFET and low-side NFET.
VIN	3	I	Input voltage supply pin. The drain terminal of high-side power NFET.
VFB	4	I	Converter feedback input. Connect to output voltage with feedback resistor divider.
EN	5	I	Enable input control. Active high and must be pulled up to enable the device.
VBST	6	O	Supply input for the high-side NFET gate drive circuit. Connect 0.1 μ F capacitor between VBST and SW pins.

$T_J = -40^{\circ}\text{C}$ to 125°C , $V_{IN} = 12\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I _{VIN}	Operating – non-switching supply current	V _{IN} current, EN = 5 V, V _{FB} = 0.8 V	TPS563201	380	520	μA
			TPS563208	590	750	
I _{VINSDN}	Shutdown supply current	V _{IN} current, EN = 0 V		1	10	μA
LOGIC THRESHOLD						
V _{ENH}	EN high-level input voltage	EN	1.6			V
V _{ENL}	EN low-level input voltage	EN			0.8	V
R _{EN}	EN pin resistance to GND	V _{EN} = 12 V	225	400	900	kΩ
V _{FB} VOLTAGE AND DISCHARGE RESISTANCE						
V _{FBTH}	V _{FB} threshold voltage	V _O = 1.05 V, I _O = 10 mA, Eco-mode™ operation		774		mV
	V _{FB} threshold voltage	V _O = 1.05 V, continuous mode operation	749	768	787	mV
I _{VFB}	V _{FB} input current	V _{FB} = 0.8 V		0	±0.1	μA
MOSFET						
R _{DS(on)h}	High-side switch resistance	T _A = 25°C, V _{BST} – SW = 5.5 V		95		mΩ
R _{DS(on)l}	Low-side switch resistance	T _A = 25°C		57		mΩ
CURRENT LIMIT						
I _{ocl}	Current limit	DC current, V _{OUT} = 1.05 V, L ₁ = 1.5 μH	3.3	4.2	5.1	A
THERMAL SHUTDOWN						
T _{SDN}	Thermal shutdown threshold ⁽¹⁾	Shutdown temperature		172		°C
		Hysteresis		37		
ON-TIME TIMER CONTROL						
t _{OFF(MIN)}	Minimum off time	V _{FB} = 0.5 V		220	310	ns
SOFT START						
T _{ss}	Soft-start time	Internal soft-start time		1.0		ms
FREQUENCY						
F _{sw}	Switching frequency	V _{IN} = 12 V, V _O = 1.05 V, FCCM mode		580		kHz
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V _{UVP}	Output UVP threshold	Hiccup detect (H > L)		65%		
T _{HICCUP_WAIT}	Hiccup on time			1.8		ms
T _{HICCUP_RE}	Hiccup time before restart			15		ms
UVLO						
UVLO	UVLO threshold	Wake up VIN voltage		4.0	4.3	V
		Shutdown VIN voltage	3.3	3.6		
		Hysteresis VIN voltage		0.4		

Electrical Characteristics

Table 8: Functional Pin Description & Electrical Characteristics

E. JW5361M (U6)

Features

- 4.5V to 18V operating input range
- 3A output current
- Up to 95% efficiency
- FCCM at light load (JW5361FM)
- PFM at light load (JW5361M)
- 600kHz switching frequency
- Internal soft-start
- Input under-voltage lockout
- Current run-away protection

- Output short protection
- Thermal protection
- Available in SOT23-6 package

<i>V_{IN}</i> =12V, <i>T_A</i> =25 °C, Unless otherwise stated.						
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
V _{IN} Under Voltage Lockout Threshold	V _{IN_MIN}	V _{IN} rising		4.2		V
V _{IN} Under voltage Lockout Hysteresis	V _{IN_MIN_HYST}			350		mV
Shutdown Supply Current	I _{SD}	V _{EN} =0V			1	μA
Supply Current	I _Q	V _{EN} =5V, V _{FB} =1V			220	μA
Feedback Voltage	V _{FB}	T _J =25 °C		765		mV
		T _J =−40 °C~125 °C		765		mV
Top Switch Resistance	R _{DS(ON)T}			80		mΩ
Bottom Switch Resistance	R _{DS(ON)B}			45		mΩ
Top Switch Leakage Current	I _{LEAK_TOP}	V _{IN} =18V, V _{EN} =0V, V _{SW} =0V			1	μA
Bottom Switch Leakage Current	I _{LEAK_BOT}	V _{IN} =18, V _{EN} =0V, V _{SW} =18V			1	μA
Bottom Switch Current Limit	I _{LIM_BOT}			3.5		A
Negative Current Limit	I _{LIM_Neg}	(JW5361FM)		-1.5		A
Minimum On Time ⁵⁾	T _{ON_MIN}			120		ns
Minimum Off Time	T _{OFF_MIN}	V _{FB} =0.4V		150		ns
Maximum On Time	T _{ON_Max}			4		us
EN Rising Threshold	V _{EN_H}	V _{EN} rising		1.2	1.3	V
EN Falling Threshold	V _{EN_L}	V _{EN} falling	0.98	1.05		V
Soft-Start Period ⁵⁾⁶⁾	t _{SS}			1.4		ms
Frequency	f _{SW}			600		kHz
Thermal Shutdown ⁵⁾	T _{TSD}			160		°C
Thermal Shutdown Hysteresis ⁵⁾	T _{TSD_HYST}			20		°C

Table 9: Electrical Characteristics

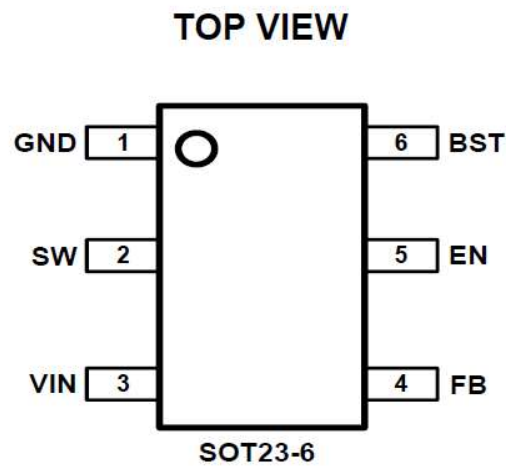


Figure 15: Pin Description

SOT23-6	Name	Description
1	GND	Ground pin.
2	SW	SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load.
3	VIN	Input voltage pin. VIN supplies power to the IC. Connect a 4.5V to 18V supply to VIN and bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC.
4	FB	Output feedback pin. FB senses the output voltage and is regulated by the control loop to 0.765V. Connect a resistive divider at FB.
5	EN	Drive EN pin high to turn on the regulator and low to turn off the regulator.
6	BST	Connect a 0.1 μ F capacitor between BST and SW pin to supply voltage for the top switch driver.

Table 10: Pin functions

F. MP1470HGJ (U16)

Features

- Wide 4.5V-to-16V Operating Input Range
- 110m Ω /57m Ω Low-RDS(ON) Internal Power MOSFETs
- Proprietary Switching-Loss-Reduction Technique
- High-Efficiency Synchronous-Mode Operation
- Fixed 1MHz Switching Frequency at CCM mode
- Internal AAM Power-Save Mode for High Efficiency at Light Load Internal Soft-Start
- Over-Current Protection and Hiccup
- Thermal Shutdown
- Output Adjustable from 0.8V
- Available in a 6-pin TSOT-23 package

PACKAGE REFERENCE

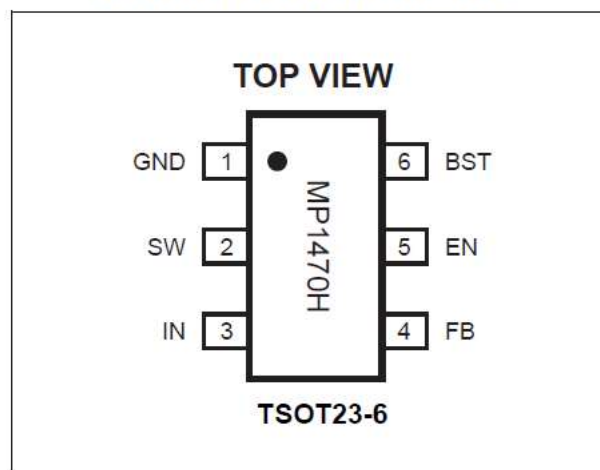


Figure 16: Pin configuration

Package Pin #	Name	Description
1	GND	System Ground. Reference ground of the regulated output voltage: requires extra care during PCB layout. Connect to GND with copper traces and vias.
2	SW	Switch Output. Connect using a wide PCB trace.
3	IN	Supply Voltage. The MP1470H operates from a 4.5V-to-16V input rail. Requires C1 to decouple the input rail. Connect using a wide PCB trace.
4	FB	Feedback. Connect to the tap of an external resistor divider from the output to GND to set the output voltage. The frequency fold-back comparator lowers the oscillator frequency when the FB voltage drops below 140mV to prevent current-limit runaway during a short circuit fault.
5	EN	EN=HIGH to enable the MP1470H. For automatic start-up, connect EN to V _{IN} using a 100kΩ resistor.
6	BST	Bootstrap. Connect a capacitor and a resistor between SW and BST pins to form a floating supply across the high-side switch driver. Use a 1μF BST capacitor.

Table 11: Functional Pin Description

V_{IN}=12V, T_A=25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Current (Shutdown)	I _{IN}	V _{EN} = 0V			1	μA
Supply Current (Quiescent)	I _q	V _{EN} = 2V, V _{FB} = 1V		0.83		mA
HS Switch-On Resistance	HS _{RDS-ON}	V _{BST-SW} =5V		110		mΩ
LS Switch-On Resistance	LS _{RDS-ON}	V _{CC} =5V		57		mΩ
Switch Leakage	SW _{LKG}	V _{EN} = 0V, V _{SW} =12V			1	μA
Current Limit	I _{LIMIT}	Duty=40%	3	4		A
Oscillator Frequency	f _{SW}	V _{FB} =0.75V	850	1000	1250	kHz
Maximum Duty Cycle	D _{MAX}	V _{FB} =700mV		87		%
Minimum On Time ⁽⁶⁾	T _{ON_MIN}			60		ns
Feedback Voltage	V _{FB}		788	804	820	mV
EN Rising Threshold	V _{EN_RISING}		1.4	1.5	1.6	V
EN Falling Threshold	V _{EN_FALLING}		1.23	1.32	1.41	V
EN Input Current	I _{EN}	V _{EN} =2V		1.8		μA
		V _{EN} =0		0		μA
V _{IN} Under-Voltage Lockout Threshold—Rising	INUV _{Vth}		3.9	4.15	4.4	V
V _{IN} Under-Voltage Lockout Threshold Hysteresis	INUV _{HYS}			340		mV
Soft-Start Period	T _{SS}	V _{out} from 0% to 100%		1.5		ms
Thermal Shutdown ⁽⁶⁾				150		°C
Thermal Hysteresis ⁽⁶⁾				20		°C

Table 12: Electrical Characteristics

G. APL5910 (U7)

- Ultra Low Dropout
- 0.12V (Typical) at 1A Output Current
- 0.8V Reference Voltage
- High Output Accuracy

- $\pm 1.5\%$ over Line, Load, and Temperature Range

- Fast Transient Response
- Adjustable Output Voltage
- Power-On-Reset Monitoring on Both VCNTL and VIN Pins
- Internal Soft-Start
- Current-Limit and Short Current-Limit Protections
- Thermal Shutdown with Hysteresis
- Open-Drain VOUT Voltage Indicator (POK)
- Low Shutdown Quiescent Current ($< 30\text{mA}$)
- Shutdown/Enable Control Function
- Simple SOP-8P Package with Exposed Pad
- Lead Free and Green Devices Available (RoHS Compliant)

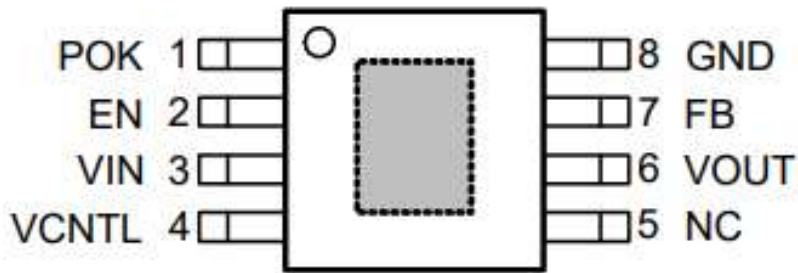


Figure 17: Pin configuration

Symbol	Parameter	Test Conditions	APL5910			Unit		
			Min.	Typ.	Max.			
SUPPLY CURRENT								
I _{VCNTL}	VCNTL Supply Current	EN=VCNTL, I _{OUT} =0A	-	1.0	1.5	mA		
I _{SD}	VCNTL Supply Current at Shutdown	EN=GND	-	20	30	μA		
	VIN Supply Current at Shutdown	EN=GND, V _{IN} =5.5V	-	-	1	μA		
POWER-ON-RESET (POR)								
	Rising VCNTL POR Threshold		2.5	2.7	2.9	V		
	VCNTL POR Hysteresis		-	0.4	-	V		
	Rising VIN POR Threshold		0.8	0.9	1.0			
	VIN POR Hysteresis		-	0.5	-	V		
OUTPUT VOLTAGE								
V _{REF}	Reference Voltage	FB=VOUT, I _{OUT} =10mA, T _J =25°C	0.792	0.8	0.808	V		
	Output Voltage Accuracy	I _{OUT} = 0~1A, T _J = -40~125 °C	-1.5	-	+1.5	%		
	Load Regulation	I _{OUT} =0A ~1A	-	0.06	0.15	%		
	Line Regulation	I _{OUT} =10mA, V _{CNTL} = 3.0 ~ 5.5V	-0.15	-	+0.15	%/V		
	VOUT Pull-Low Resistance	V _{CNTL} =3.3V, V _{EN} =0V, V _{OUT} <0.8V	-	85	-	Ω		
	FB Input Current	V _{FB} =0.8V	-100	-	100	nA		
DROPOUT VOLTAGES								
V _{DROP}	VIN-to-VOUT Dropout Voltage	V _{CNTL} =4.5V, I _{OUT} =1A	V _{OUT} =2.5V	T _J =25°C	-	0.13	0.16	V
				T _J =-40~125°C	-	-	0.22	
			V _{OUT} =1.8V	T _J =25°C	-	0.12	0.15	
				T _J =-40~125°C	-	-	0.20	
			V _{OUT} =1.2V	T _J =25°C	-	0.12	0.14	
				T _J =-40~125°C	-	-	0.19	
Symbol	Parameter	Test Conditions	APL5910			Unit		
			Min.	Typ.	Max.			
PROTECTIONS								
I _{LIM}	Current-Limit Level	T _J =25°C	1.7	2.1	2.5	A		
		T _J = -40 ~ 125°C	1.4	-	-			
I _{SHORT}	Short Current-Limit Level	V _{FB} <0.2V	-	0.4	-			
	Short Current-Limit Blanking Time	From beginning of soft-start	0.6	1.6	-	ms		
T _{SD}	Thermal Shutdown Temperature	T _J rising	-	170	-	°C		
	Thermal Shutdown Hysteresis		-	50	-	°C		
ENABLE AND SOFT-START								
	EN Logic High Threshold Voltage	V _{EN} rising	0.5	0.8	1.1	V		
	EN Hysteresis		-	80	-	mV		
	EN Pull-High Current	EN=GND	-	5	-	μA		
T _{SS}	Soft-Start Interval		0.3	0.6	1	ms		
POWER-OK AND DELAY								
V _{THPOK}	Rising POK Threshold Voltage	V _{FB} rising	90	92	94	%		
	POK Threshold Hysteresis		-	8	-	%		
	POK Pull-Low Voltage	POK sinks 5mA	-	0.25	0.4	V		
	POK Debounce Interval	V _{FB} <falling POK voltage threshold	-	10	-	μs		
	POK Delay Time	From V _{FB} =V _{THPOK} to rising edge of the V _{POK}	1	2	4	ms		

Table 13: Electrical Characteristics

6. MICROCONTROLLER

NOVATEK NT72564 (U19)

The NT72564 is an integrated digital TV system-on-chip which complies with variety ATV as NTSC, PAL and SECAM, and DTV standards as ISDB-T, DVB-T/-T2/-C/-S/-S2, ITU-T J.83B, ATSC, integrates DTV and multi-media AV decoder, SIF demodulator, and support A/V post-processing.

The integrated video ADC and video decoder support PC VGA port, YPbPr/CVBS input. Regarding the tuner input, the digital VIF performs the universal analog TV demodulation (NTSC, PAL, and SECAM), including IF processing, AGC, video demodulation, and second sound IF generation (SSIF). The video decoder supports universal TV video format. The integrated audio ADC supports stereo audio input corresponding to video input sources. The integrated TV sound decoder supports universal TV sound format.

The advanced picture quality and color engine create more vivid image impression than ever. The HDMI receiver v1.4b, supports deep color, CEC features and 3D formats, eARC transmitter functions are supported as well. The USB high speed host supports updating firmware code, multi-media playback from the external USB flash devices.

The standby controller can operate solely from the main system, powered by the standby power source from power module, consumes as low current as possible. It meets the requirement of Green appliance.

CPU

- ARM CA53 Quad-core
- Support TrustZone
- Support PTM
- Support NEON

DRAM Interface

- DDR 3 32bit MCP
- Spread Spectrum PLL for EMI reduction

Flash controller

- NAND type flash (3V3 not boot device)
- RS/BCH Support
- eMMC 4.51 with HS200 type flash
- SPI NOR type flash x 1 Supports dual stream decoding for 3D content

Stand by Controller

- Supports VGA / IR / KeyPad / CEC/ wake up
- Built in Turbo 8051 for stand by application usage
- Built in Low Voltage Reset for brown out
- Built in EDID for saving system BOM cost
- System power control

Condition Access

- Support Common Interface
- Support Common Interface Plus
- Built in Cryptograph Engine for conditional access and CI Plus
- Meet Common Interface Plus's Robust and Compliance rule

Copy Protection Engine

- Support Cryptograph Key Protection
- Support Demux Key Protection
- Support HDCP Key Protection

Internal High Speed Video ADC

- Integrated triple high speed ADCs/ PLL to support both YPbPr and RGB format signal
- 10 bits data resolution
- Maximum conversion up to 165 MSPS
- Support 0.7 ~ 1.0 Volts analog RGB/YUV input
- 2 : 1 analog input MUX
- Supports both non interlaced and interlaced input signals

Analog Video Decoder

- Clamp and AGC (Automatic Gain Control) circuit to support 0.5 to 1.6V analog input signal
- Support multi standards, macro vision detection and related status report
- Embedded Teletext Level 2.5 / Close Caption and other VBI Decoder
- 2D and 3D adaptive Comb Filter for better Y/C Separation
- Support VPS signal decode for EU channel sorting purpose

TV encoder with built in video DAC

- Built in 10 bit DAC for CVBS Analog Video output.
- Support TTX/ CC/ WSS/ VPS/ CGMS A/ Macrovision insertion

Digital Video CODEC

- Built-in multi-standard video codec
- Support pixel format YUV420 only for all video codec except JPEG
- H.264 Constrained Baseline/Main/High Profiles @ 1080p60 (Level 4.0 and Level 4.1 under limited bit-rate)
- VP8 Profiles @ 1080p30
- VP9 Profile 0, 2 up to 10-bit @ 1080p60
- AV1 Main profile @ 1080p60 (under limited bit-rate and resolution)
- AVS(Optional)Jizhun Profile @ 1080p30 (Level 6.0)
- AVS+(Optional)@ 1080p30
- VC-1(Optional)Simple/Main/AdvancedProfiles @ 1080p30 (Level 3.0)
- RealVideo(Optional)8/9/10@ 1080p30
- MPEG-4 Simple/Advanced Simple Profiles @ 1080p30
- H.263 Profile 0 @ 1080p30
- Sorenson Spark @ 1080p30
- MPEG-2 Main Profile @ 1080p30
- MPEG-1 @ 1080p30
- JPEG baseline sequential mode
- Support pixel formats in YUV420, YUV422 and YUV444
- Support Motion JPEG @ 1080p30
- HEVC(H.265) Main 10 profile @1080p60(level4.1)

De Interlacing

- Support progressive scan 24Hz to 85Hz Frame Rate Conversion

- 5th generation High performance Motion-Adaptive De-interlacing
- 5th generation Diagonal Edge Enhancement for smoothing edge outline
- Automatic Video Source Detection
- Support Inverse 3:2/2:2 pull down and multiple cadence for film stream
- Scene Change Detection
- Built-in Anti-Crosscolor to remove abnormal color performance
- Built-in Color Performance stabilizer for SECAM video format
- Built-in Region Classifier engine to get flicker free image quality

Visual Effect Processor

- Built-in Advanced Super Resolution
- 5th generation Advanced Scaling Up Engine
- Support Nonlinear Scaling
- 5th generation LTI/CTI function
- Support 5th Color Engine
- Global Brightness, Contrast, Hue Saturation and Intensity Adjustment
- Built-in I-Gamma and Black Stretch for Automatic Contrast Adjustment
- Support sRGB and xvYCC Adjustment Standard
- De-blocking, De-Mosquito, Temporal and Spatial Noise Filter
- Adaptively determine 3D noise filter for different noise level
- Linear Gamut Remapping
- SD2HD detection and Processing
- DP Meter for Dynamic backlight Control
- Support HDR
- Support Cinema Contrast Enhancer2.0

Display Processor

- Embedded dual 10 bit LVDS transmitter
- Supports single pixel / dual pixel output
- Dithering function supports 30-bit quality for 24 bit or 18-bit panel
- Optional Frame Sync or Free Run display synchronization modes
- Display Resolution up to 1920X1080@60Hz HDTV format
- Built-in Gamma Correction for different type display device
- Supports Pivot (H flipping display)
- V flipping is in LBM
- Support H/V sync out
- Video alpha blending

3D Graphic Engine

- Mali-G52-2EE MC1
- Support the MMU function
- Supports OpenGL ES 1.x & 2.0,
- Supports OpenVG 1.0 & 1.1

2D Graphic Engine

- Bitmap Operation
- ARGB/RGBA format
- Copy/Color expansion
- Logic Operation
- Copy with alpha blending (only 16/32 bit color mode)
- Source and destination area could be overlapped
- Color key for the transparency effect
- 12 Raster Operation (ROP) rules
- Fill Rectangle
- Color fill
- Gradient fill
- Scaling
- Bicubic Algorithm

OSD

- 8/16/32-bit OSD Architecture
- 2 OSD Layers
- 5 levels of transparency with pixel or frame based operation (background, video, Plane2, Plane1, cursor)
- Programmable width & height to meet LCD/TV's resolution exactly
- H/V scaling

HDMI receiver

- 3 HDMI Input ports
- HDMI Rx 1.4b Compliant
- Integrated HDCP 1.4 & 2.2 cipher engine for Content Protection
- Support High-Level CEC Command for Easy Link between CE equipments.
- Support Deep Color for more pixel depth information
- Support xvYCC for wide color gamut application
- 3D support
- Support Audio format including
- 2~8 channels, 32-192 KHz
- Support ARC (Audio Return Channel)
- Support Multi-VSIF
- Support eARC TX (Enhanced Audio Return Channel)

SIF Demodulator

- NICAM-BG/DK/I/L, A2-BG/DK/I, BTSC, A2-M, AM SECAM-L
- Automatic standard and mode detection
- Automatic carrier mute and automatic NICAM fall back
- 32 KHz audio output

Audio CODEC (Audio ADC/DAC)

- Built-in 1 audio ADC input mux (MAX. sampling rate 48 KHz)
- Built-in 1 audio DAC output (MAX. sampling rate 48 KHz)
- Built-in 2 I2S Output format for Power-Stage Amplifier
- S/PDIF output supported

Audio Processor

- Dedicated DSP to decode compressed audio
- Supports digital audio format decoding:
 - MPEG-1/2 (Layer I/ II/ III), Dolby Digital (AC3) (Optional), Dolby Digital Plus (EAC3) (Optional), AC4 (Optional), TrueHD (Optional), AAC-LC (Optional), HE-AAC (Optional), WMA3 (Optional), WMA (Optional), DTS (Optional)
- Supports Dolby MS12 (Optional) multistream decoder, including Dolby Digital Encoder for transcoding streams to Dolby Digital 5.1
 - Support DTS M6 (Optional)
- Supports DTS Neo 2:5 (Optional) to transcoding streams to DTS 5.1
- Advance sound processing: Automatic Volume Control, 5-band EQ, Automatic Gain Control, Virtual Surround, Dynamic range control (DRC)
 - Advance sound processing options available, for example: DTS TruSurround HD (Optional), DTS Studio Sound (Optional), DTS Virtual:X (Optional)

Digital VIF Demodulator

- Compliant with NTSC, PAL, SECAM video standards for universal analog terrestrial and cable support
- Support for FM-A2 (IRT-A2), AM, BTSC+SAP, MK-A2, NICAM audio standards
- Support Low IF, 5 ~ 8 MHz (silicon tuner)
- Single IF AGC control with $\Delta\Sigma$ modulation
- Flexible channel bandwidth (6 MHz, 7 MHz, and 8 MHz)
- Digital video and audio dual-path split processor

ISDB-T Demodulator

- Compliant with ISDB-T standard ARIB STD-B31 and SBTVD standard ABNT NBR 15601
- Receiver specifications ARIB STD-B21 & ABNT NBR 15604 fulfilled
- Channel bandwidth 6, 7 & 8 MHz supported
- Low IF with configurable mixing frequency
- Single IF AGC controls with $\Delta\Sigma$ modulation
- Partial (1-segment) & full (13-segment) reception supported
- Non-hierarchical (single-layer) & hierarchical (layers A/B/C) reception supported
- Automatic detection of transmission parameters:
- Modes 1 (2k), 2 (4k), 3 (8k)
- Guard intervals of 1/4, 1/8, 1/16, 1/32
- Constellations DQPSK, QPSK, 16QAM, 64QAM
- Code rates of 1/2, 2/3, 3/4, 5/6, 7/8
- Start flag for emergency-alarm broadcasting
- Robust TMCC decoding
- Impulsive noise reduction
- Adjacent-channel interference suppression
- Superior AWGN & SFN performance
- Superior co-channel interference performance
- Timing acquisition range: ± 100 ppm
- Carrier acquisition range: ± 400 kHz (6 MHz bandwidth)
- Performance monitoring: SNR (dB), pre-Viterbi BER, post-Viterbi BER, RS uncorrectable error count

DVB-T Demodulator

- Compliant with ETSI EN 300 744, NorDig Unified 2.5.1, D-Book 7 Part A v3, and Digtene 4.0.4 fulfilled
- Channel bandwidth 6, 7 & 8 MHz supported
- Low-IF with configurable mixing frequency
- Single IF AGC control with $\Delta\Sigma$ modulation
- Non-hierarchical & hierarchical (high-priority / low-priority) reception supported
- Automatic detection of transmission parameters:
- 2K/8K modes
- Guard intervals of 1/4, 1/8, 1/16, 1/32
- Constellations QPSK, 16QAM, 64QAM
- Code rates of 1/2, 2/3, 3/4, 5/6, 7/8
- Robust TPS decoding
- Impulsive noise reduction
- Adjacent channel interference (ACI) filter and Co-channel interference (CCI) suppression
- Superior AWGN & SFN performance
- Timing acquisition range: ± 100 ppm

- Carrier acquisition range: ± 650 kHz (8 MHz bandwidth)
- Performance monitoring: SNR (dB), pre-Viterbi BER, post-Viterbi BER, RS uncorrectable error count

DVB-C Demodulator

- Compliant with ETSI EN 300 429 DVB-C Receiver specifications NorDig Unified 2.2.2, Ziggo and China HD_GY/T 241-2009 fulfilled
- Low-IF with configurable mixing frequency
- Single IF AGC control with $\Delta\Sigma$ modulation
- Variable Symbol Rates supported: 1 MBaud ~ 7.2 MBaud
- Constellation supported: 16/32/64/128/256-QAM
- Matched Filters (Roll-off factor= 0.15)
- Robust blind adaptive equalizer
- Superior impulsive noise cancellation
- High monitoring capabilities
 - C/N ratio (SNR)
 - Signal Power
 - RS uncorrectable error Number

ATSC Demodulator

- ATSC A.53d compatible
- Low IF supported with configurable mixing frequency
- Single IF AGC control with $\Delta\Sigma$ modulation
- Carrier recovery with or without pilot
- Excellent ATSC 50-channel reception performance
- Excellent phase noise tracking performance
- Pass Brazil A/B/C/D/E
- Excellent CCI rejection performance
- Timing acquisition range: ± 200 ppm
- Carrier acquisition range: ± 200 kHz
- Performance monitoring: SNR, BER, RS uncorrectable error count

J.83B Demodulator

- ITU J.83B compatible
- Low IF supported with configurable mixing frequency
- Single IF AGC control with $\Delta\Sigma$ modulation
- 64/256QAM automatic detection
- Excellent phase noise tracking performance
- Excellent co-channel single tone rejection capability
- Timing acquisition range: ± 800 ppm
- Carrier acquisition range: ± 400 kHz (64QAM)
- Robust blind adaptive equalizer

- Superior impulsive noise cancellation
- Performance monitoring: SNR, BER, RS uncorrectable error count

DVB T2

- DVB-T2 standard ETSI EN 302 755 compliant
- NorDig-Unified 2.5.1 and D-Book 7 Part A v3 requirements fulfilled
- Channel BW 1.7, 5, 6, 7, 8 MHz
- All single-profile DVB-T2 modes supported, including
- T2-Base profile
- T2-Lite profile
- Single and Multiple PLPs
- SISO and MISO transmissions
- Rotated and non-rotated constellations
- Scrambled L1-post signaling
- PAPR
- FEF skipped automatically
- Low-IF supported with configurable mixing frequency
- Carrier acquisition range: ± 650 kHz @ 8 MHz BW
- Timing acquisition range: ± 100 ppm
- Automatic spectral inversion detection
- Superior Single Frequency Network performance
- Excellent co-channel interference suppression
- Fast channel zapping

DVB S/S2

- Compliant to ETSI EN 300 421 DVB-S and EN 302 307 DVB-S2 Broadcast Services
- QPSK, 8PSK, 16APSK and 32APSK
- QPSK/8PSK 1 ~ 45Msps, 16APSK: 1 ~ 39Msps and 32APSK 1 ~ 32Msps
- Blind Scan
- Differential and single end IQ input

- Dual ADC interface
- IQ mismatch removal
- Automatic spectrum inversion
- DiSEqCTM v2.2

Ethernet

- Built-in 10/100 Ethernet MAC and PHY
- Support WOL

Miscellaneous

- Built-in UART controller
- LFBGA 19x 19(415Balls)

USB host/device controller with built in transceiver

- 3USB host ports
- Compliant with USB Specification Revision 2.0
- Support high-speed, full-speed and low-speed devices
- Integrated USB 2.0 transceiver

Tcon function

- P2P TX support USIT, CEDS/EPI, ISP/CSPI, CHPI, CMPI
- Support OD
- Support Dual gamma
- Support Demurafunction

LED backlight

- PWM x 2
- PWM delay and duty is adjustable individually
- PWM delay is phase-locked to VS
- Support PWM frequency = 1 x VS , 2 x VS frequency
- SPI LED-driver interface

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
VDD_C ORE	System Core power supply	0.9215	0.97	1.0185	V	
VDD_C PU_CO RE	ARM Core power supply	0.969	1.02	1.071	V	
V1.5V	1.5V power supply (DDR3)	1.425	1.5	1.575	V	
V1.8V	1.8V power supply (eMMC)	1.7	1.8	1.9	V	
V2.5V	2.5V power supply	2.375	2.5	2.625	V	
VDDIO	3.3V power supply	3.135	3.3	3.465	V	
VIN3	3.3V I/O with 5V Tolerance	0	3.3	5	V	
	Input voltage of 3.3V I/O	0	3.3	3.465	V	

Table 14: Recommended Operating Conditions

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Core Power Supply of 0.97V	VDD	0.9215	1.0185	V
Power Supply of 3.3V I/O	VDDIO		3.465	V
Input Voltage of 3.3V I/O	VDDIO		3.465	V
Input Voltage of 3.3V I/O(5V tolerance)	VDDIO5		5	V
Operating Ambient Temperature	TA	0	+80	°C
Storage Temperature	TS	-40	+150	°C
RA Junction Temperature Tolerance	TJ(RA)	+125		°C
Power Consumption N1	Pd	TBD	TBD	W
Thermal Resistance Theta JA Junction to Air N2	ΘJA	26.8		°C/W
Thermal Resistance Psi JT N2	ΨJT	0.34		°C/W
Thermal Resistance Theta JA Junction to Air N3	ΘJA	20.9		°C/W
Thermal Resistance Psi JT N3	ΨJT	0.25		°C/W

Table 15: Absolute Maximum Ratings

7. 4 GB EMMC

SAMSUNG EMMC 4GB KLM4G1FETE-B041 (U138)

Description

SAMSUNG eMMC is an embedded MMC solution designed in a BGA package form. eMMC operation is identical to a MMC device and therefore is a simple read and write to memory using MMC protocol v5.1 which is a industry standard. eMMC consists of NAND flash and a MMC controller. 3V supply voltage is required for the NAND area (VDDF or VCC) whereas 1.8V or 3V dual supply voltage (VDD or VCCQ) is supported for the MMC controller. SAMSUNG eMMC supports HS400 in order to improve sequential bandwidth, especially sequential read performance. There are several advantages of using eMMC. It is easy to use as the MMC interface allows easy integration with any microprocessor with MMC host. Any revision or amendment of NAND is invisible to the host as the embedded MMC controller insulates NAND technology from the host. This leads to faster product development as well as faster times to market. The embedded flash management software or FTL(Flash Transition Layer) of eMMC manages Wear Leveling, Bad Block Management and ECC. The FTL supports all features of the Samsung NAND flash and achieves optimal performance.

Key Features

- Embedded MultiMediaCard Ver. 5.1 compatible.
- SAMSUNG eMMC supports features of eMMC5.1 which are defined in JEDEC Standard
- Major Supported Features : HS400, Field Firmware Update, Cache, Command Queuing, Enhanced Strobe Mode, Secure Write Protection, Partition types
- Non-supported Features : Large Sector Size (4KB)
- Backward compatibility with previous MultiMediaCard system specification (1bit data bus, multi-eMMC systems)
- Data bus width : 1bit (Default), 4bit and 8bit
- MMC I/F Clock Frequency : 0 ~ 200MHz
MMC I/F Boot Frequency : 0 ~ 52MHz
- Temperature : Operation (-25°C ~ 85°C), Storage without operation (-40°C ~ 85°C)
- Power : Interface power → VCCQ(1.70V ~ 1.95V), Memory power → VCC(2.7V ~ 3.6V)

Item	Min	Max	Unit
V _{CCQ}	1.70 (2.7)	1.95 (3.6)	V
V _{CC}	2.7	3.6	V
V _{SS}	-0.5	0.5	V

Table 16: Supply Voltage

8. USB INTERFACE

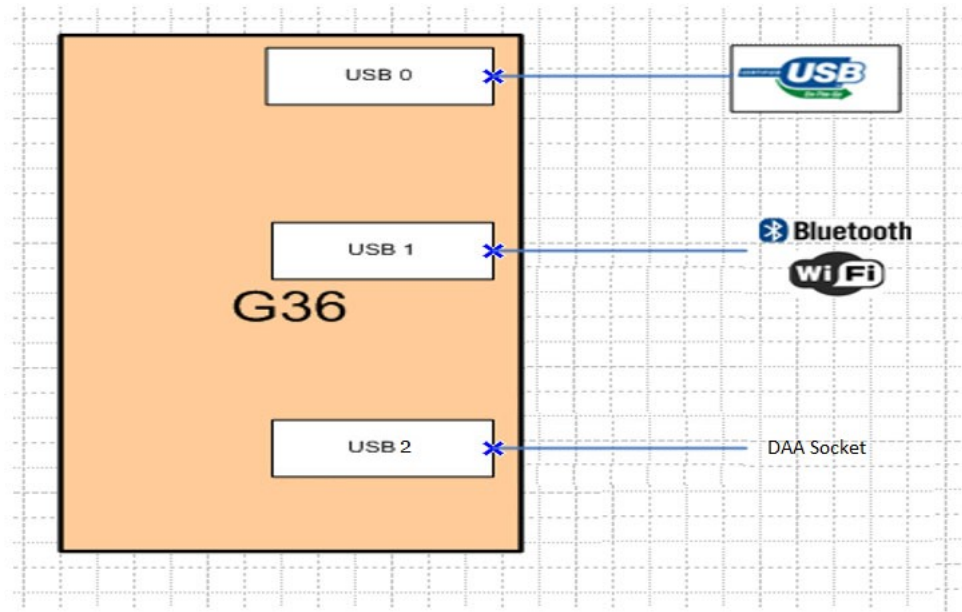


Figure 18: Block diagram of USB interface

A. USB POWER SWITCH TPS25221 (U20)

Features

- 2.5-V to 5.5-V VOPERATING
- Pin-to-Pin with TPS2553
- 2-A ICONT_MAX
- 0.275-A to 2.7-A Adjustable ILIMIT ($\pm 6.5\%$ at 1.7 A)
- 70-m Ω (typical) RON
- 1.5- μ s Short Circuit Response
- 8-ms Fault Reporting Deglitch
- Reverse Current Blocking (when disabled)
- Built-In Soft Start
- UL 60950 and UL 62368 Recognition
- 15-kV ESD Protection per IEC 61000-4-2 (with external capacitance)

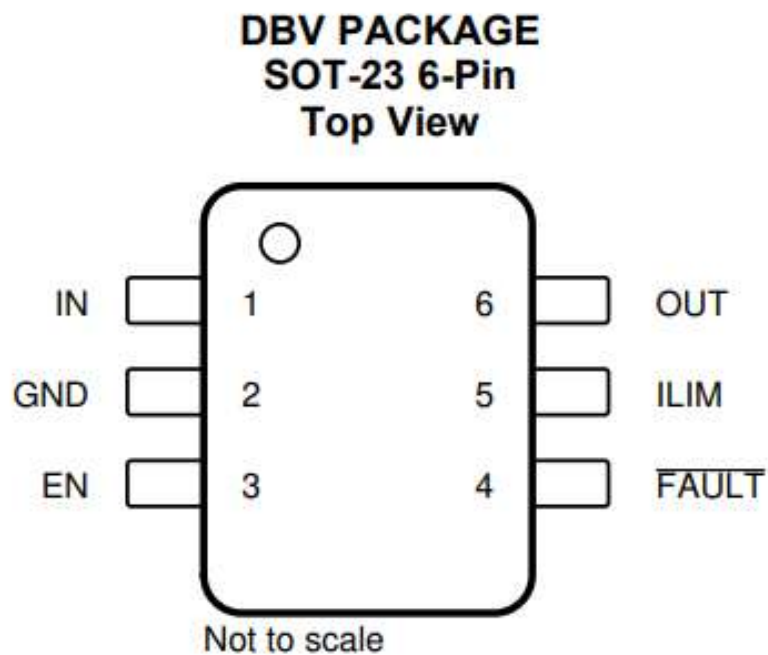


Figure 19: Pin configuration

9. CI INTERFACE

17MB281 Digital CI Interface Block diagram:

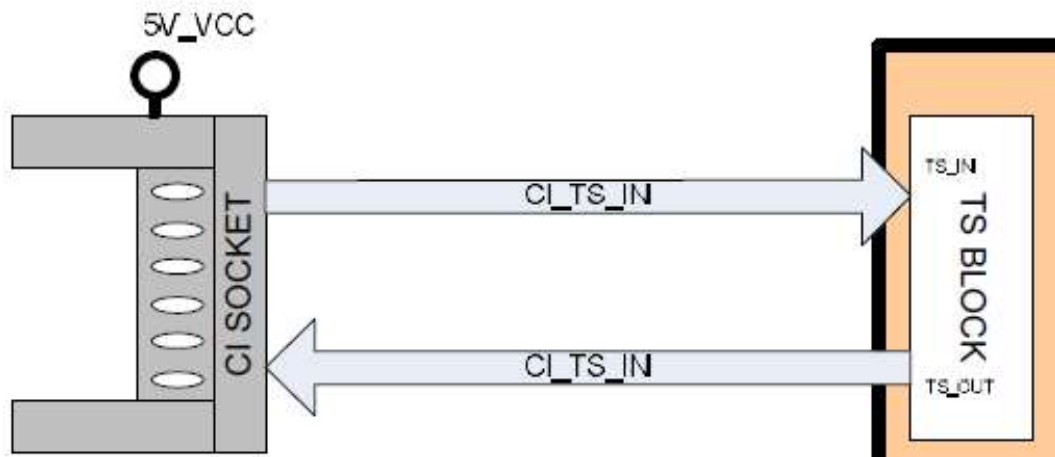


Figure 20: CI interface

10. SOFTWARE UPDATE

MAIN SOFTWARE UPDATE

In MB281 project, please follow software update procedure:

1. [sidious_usb_update.bin](#) documents should be copied directly inside root of a flash memory (not in a folder).
2. Insert flash memory to the TV when TV is powered off.
3. While pushing the OK button on remote controller, then power on and wait. TV will power-up itself.
4. If first Time Installation screen comes, it means software update procedure is successful.

11. TROUBLESHOOTING

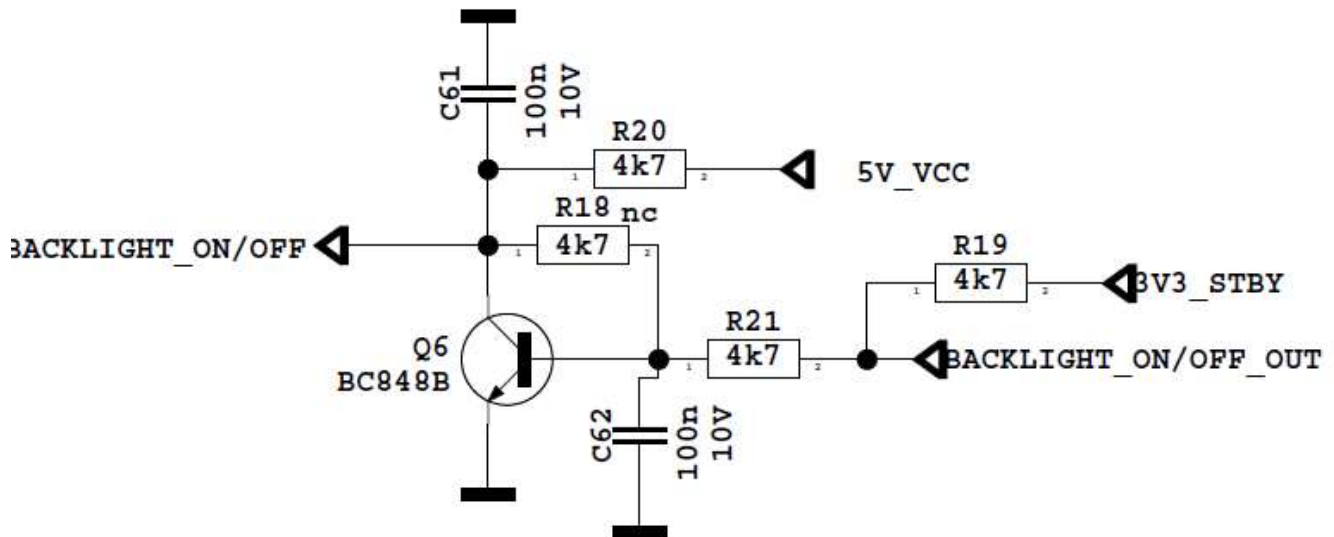
A. NO BACKLIGHT PROBLEM

Problem: If TV is working, led is normal and there is no picture and backlight on the panel.

Possible causes: Backlight pin, dimming pin, backlight supply, stby on/off pin

BACKLIGHT_ON/OFF pin should be high when the backlight is ON. Collector pin of Q6 must be low when the backlight is OFF. If it is a problem, please check Q3. Also it can be tested in TP4 in main board. Please also check panel cables.

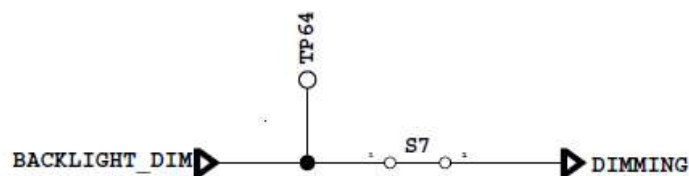
Backlight On/Off Circuit



Dimming pin should be high or square wave in open position. It also can be checked at TP3. Please also check panel or power cables and connectors.

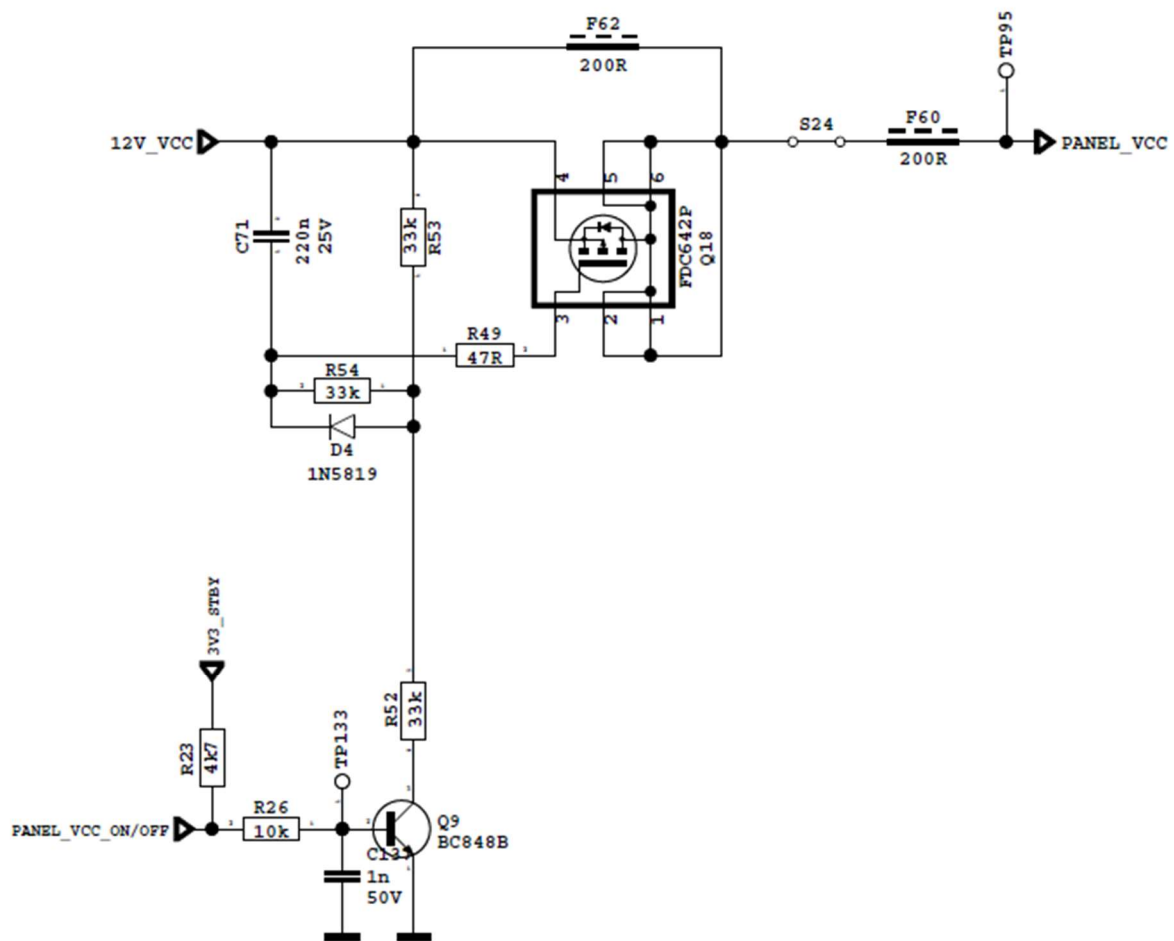
Backlight power supply should be in panel specs. Please check Q18, shown below; also it can be checked TP95.

DIMMING



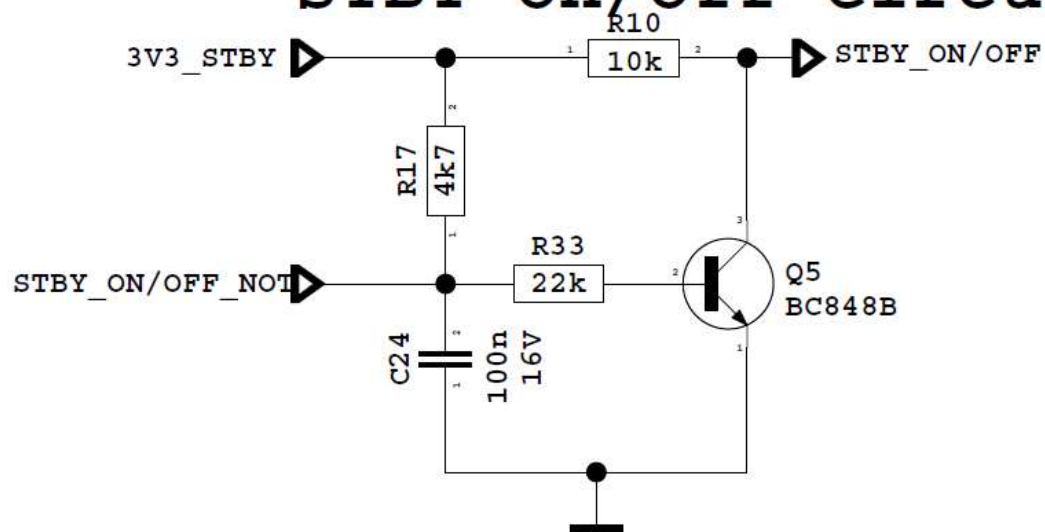
PANEL SUPPLY SWITCH

common



STBY_ON/OFF_NOT should be low for TV on condition, please check Q5's collector.

STBY On/Off Circuit

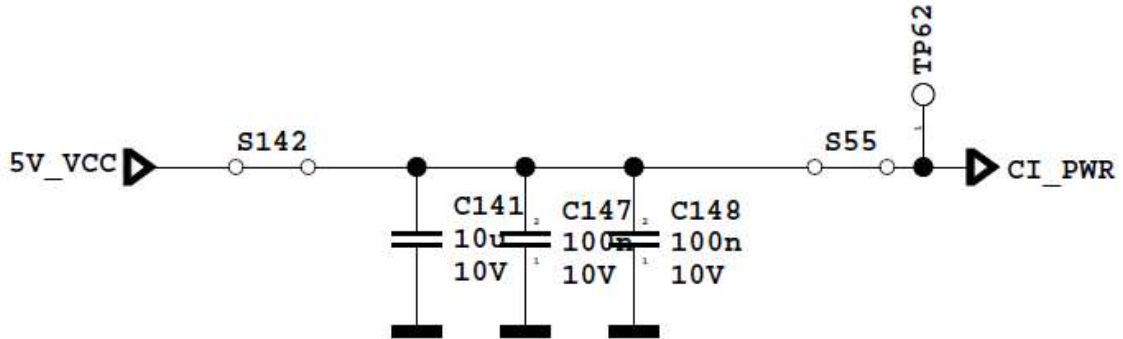


B. CI MODULE PROBLEM

Problem: CI is not working when CI module inserted.

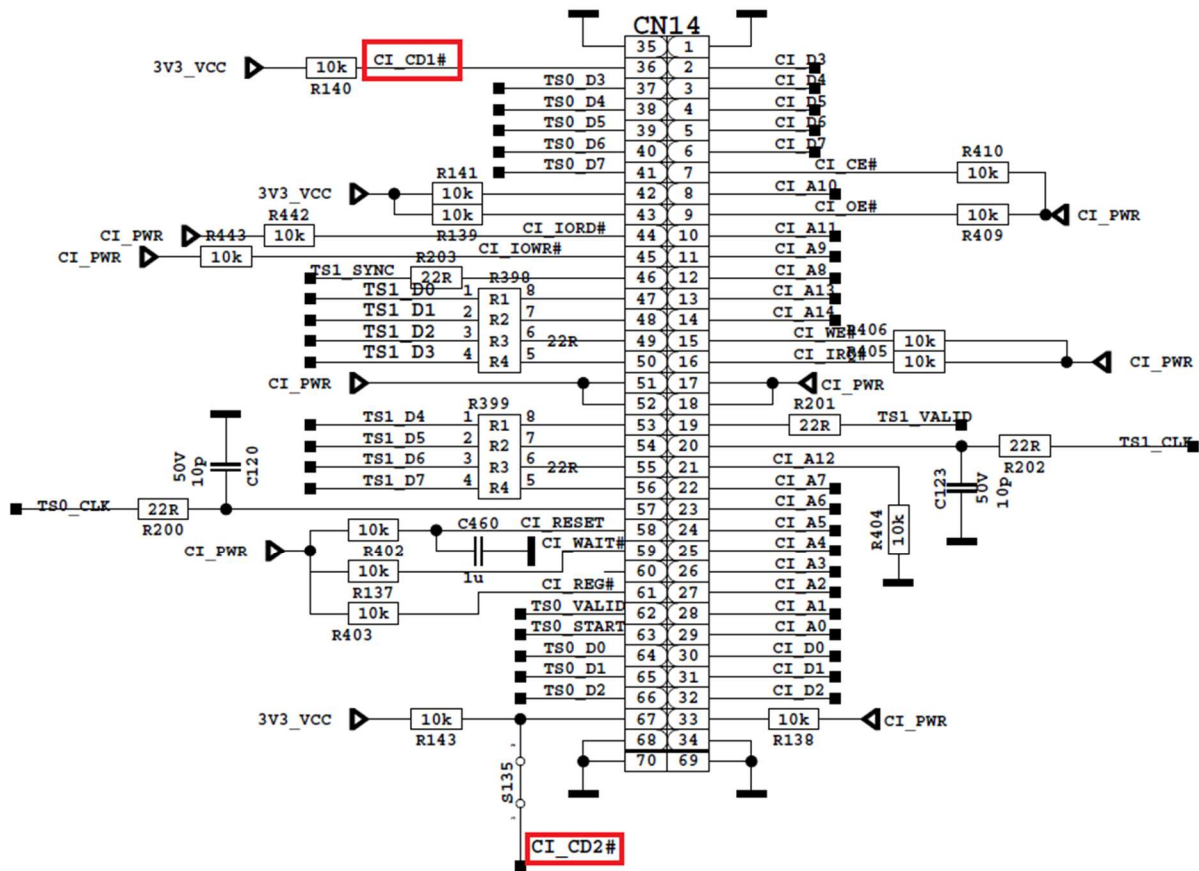
Possible causes: Supply, supply control pin, detects pins, mechanical positions of pins.

- CI supply should be 5V when CI module inserted.



- Please check mechanical position of CI module. Is it inserted properly or not?
- Detect ports should be low. If it is not low please check CI connector pins, CI module pins.

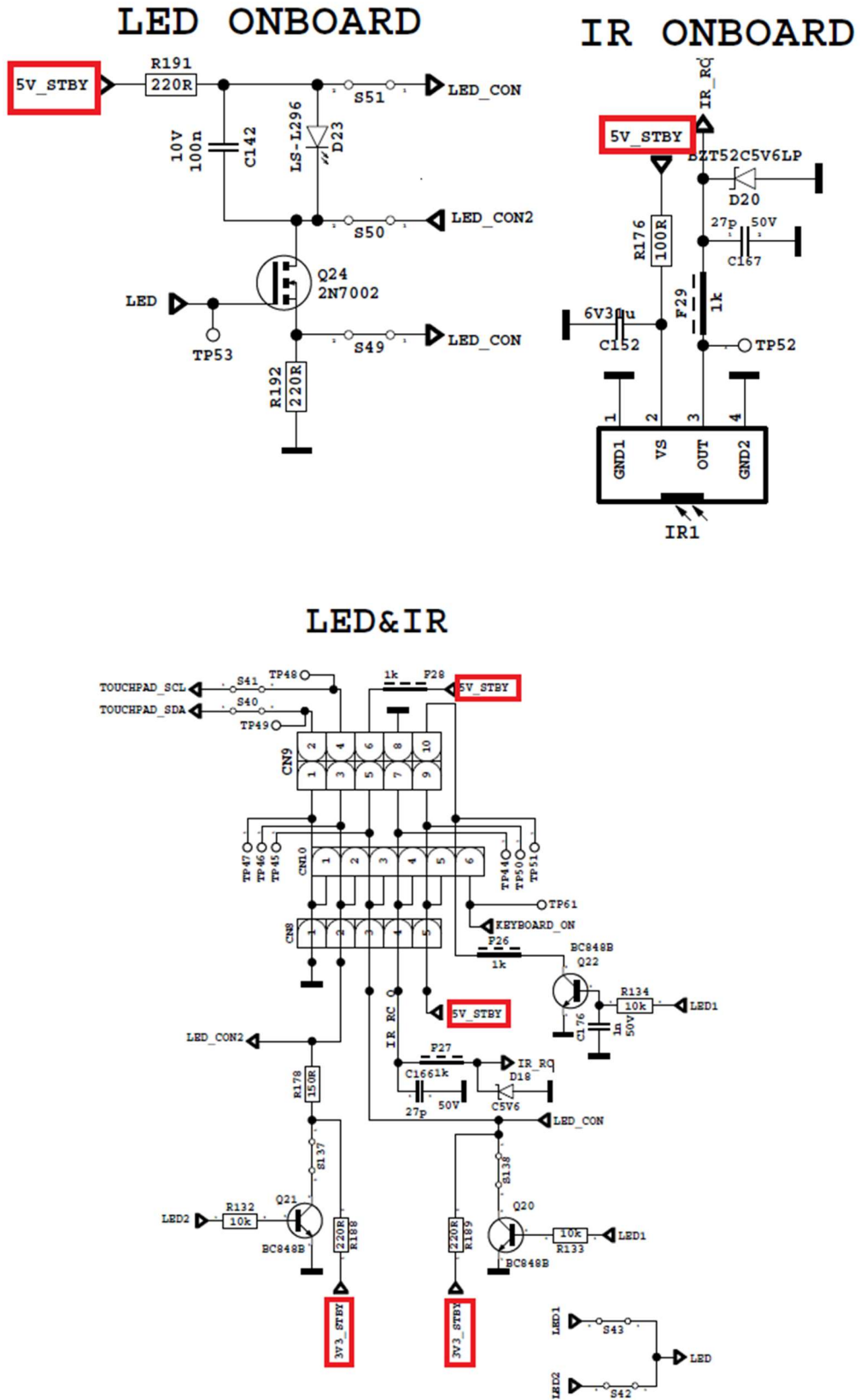
CI



C. IR PROBLEM

Problem: LED or IR not working

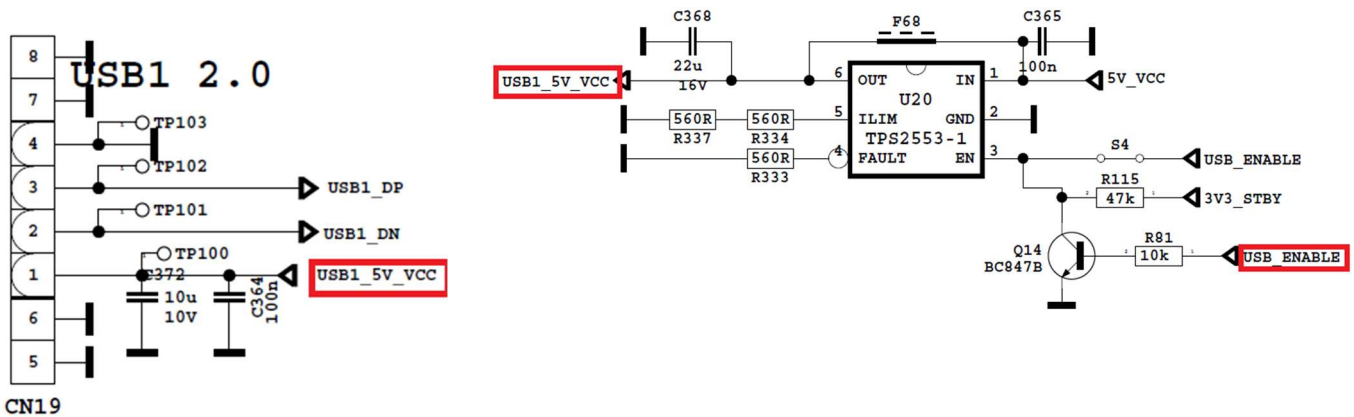
Check LED card supply on MB281 chasis.



D. USB PROBLEMS

Problem: USB is not working or no USB Detection.

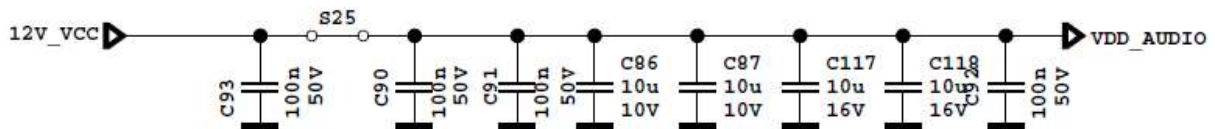
Check USB Supply, It should be nearly 5V. Also USB Enable should be logic high.

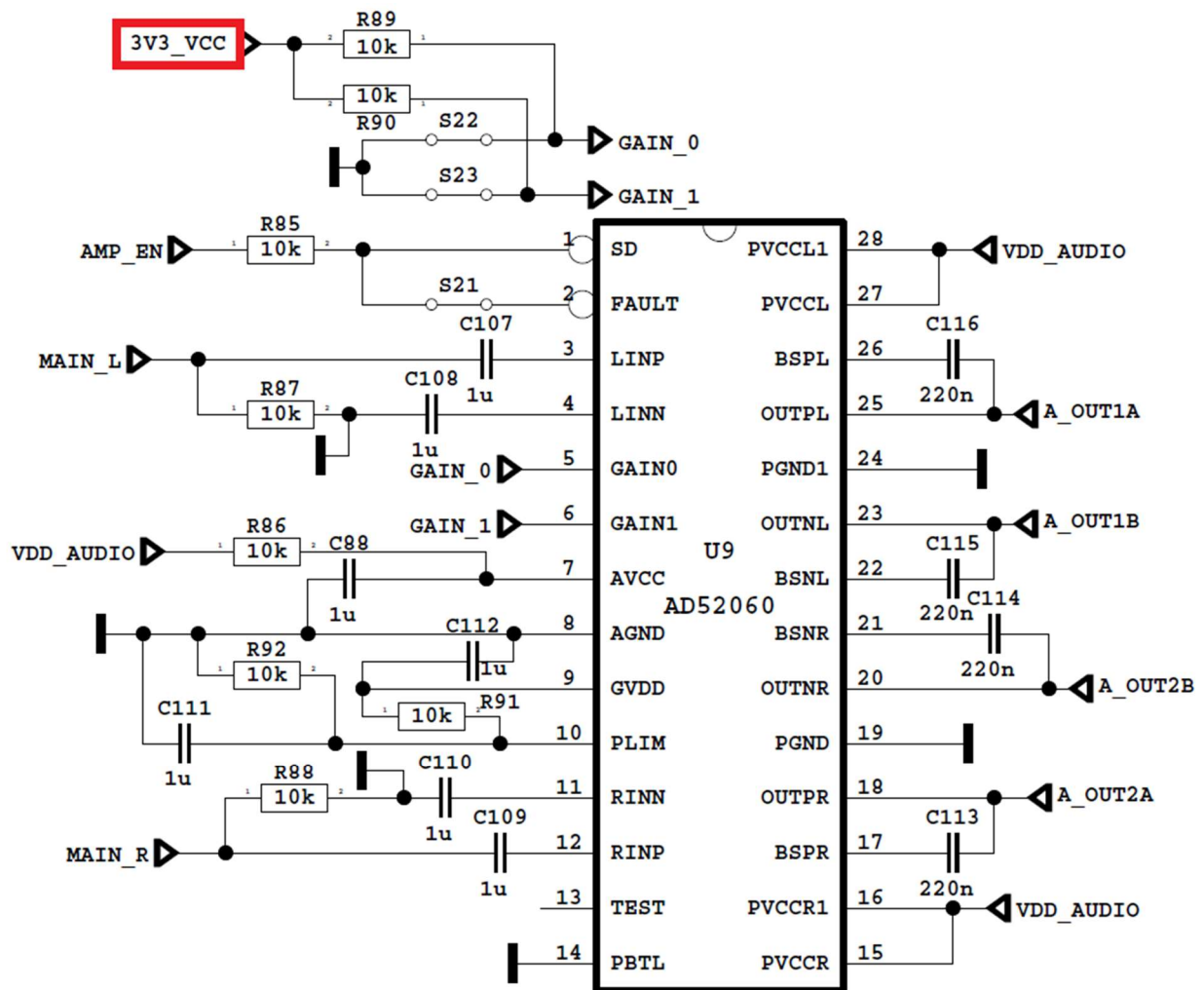


E. NO SOUND PROBLEM

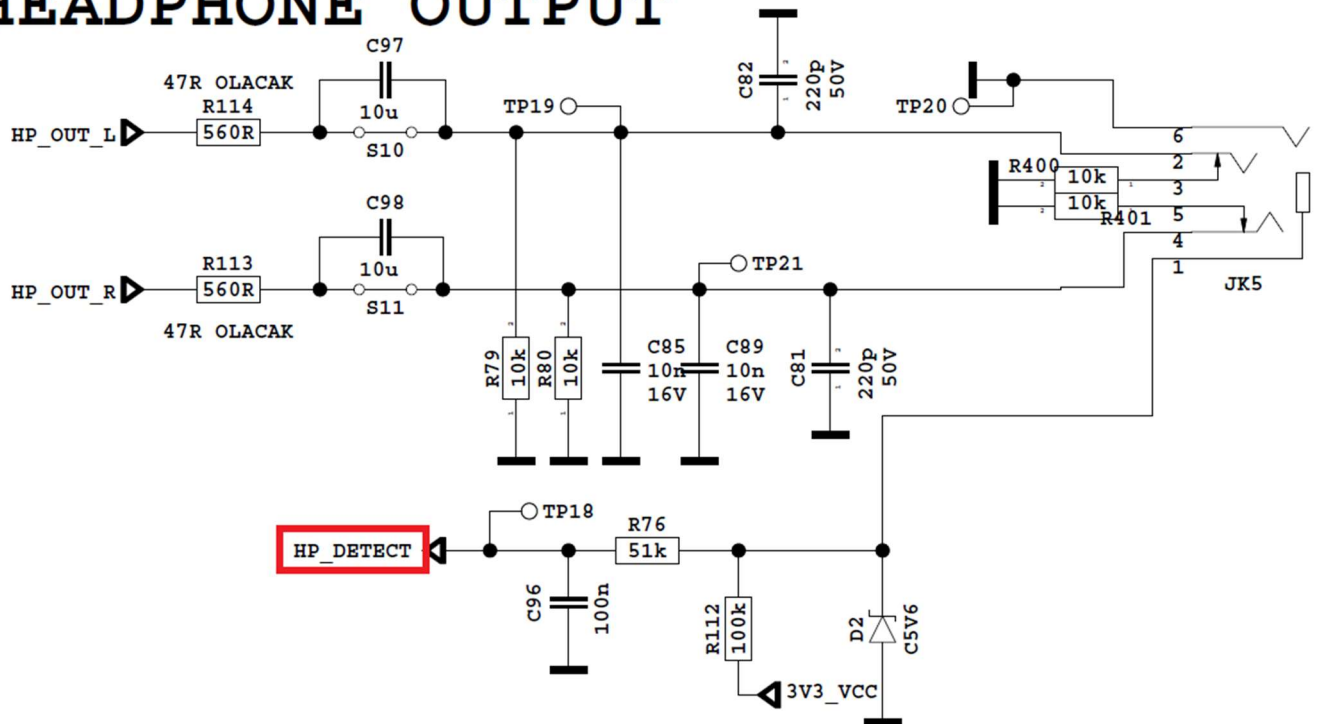
Problem: No audio at main TV speaker outputs.

Check supply voltages of 12V_VCC, VDD_AUDIO and AMP_EN with a voltage-meter. There may be a problem in headphone connector or headphone detect circuit. Measure voltage at HP_DETECT pin, it should be 3.3v if there is a problem.





HEADPHONE OUTPUT



F. STANDBY ON/OFF PROBLEM

Problem: Device cannot boot, TV hangs in standby mode.

There may be a problem about power supply. Check main supplies with a voltage-meter. Also there may be a problem about SW. Try to update TV with latest SW. Additionally it is good to check SW printouts via Teraterm program. These printouts may give a clue about the problem. You can use VGA for Teraterm program connection.

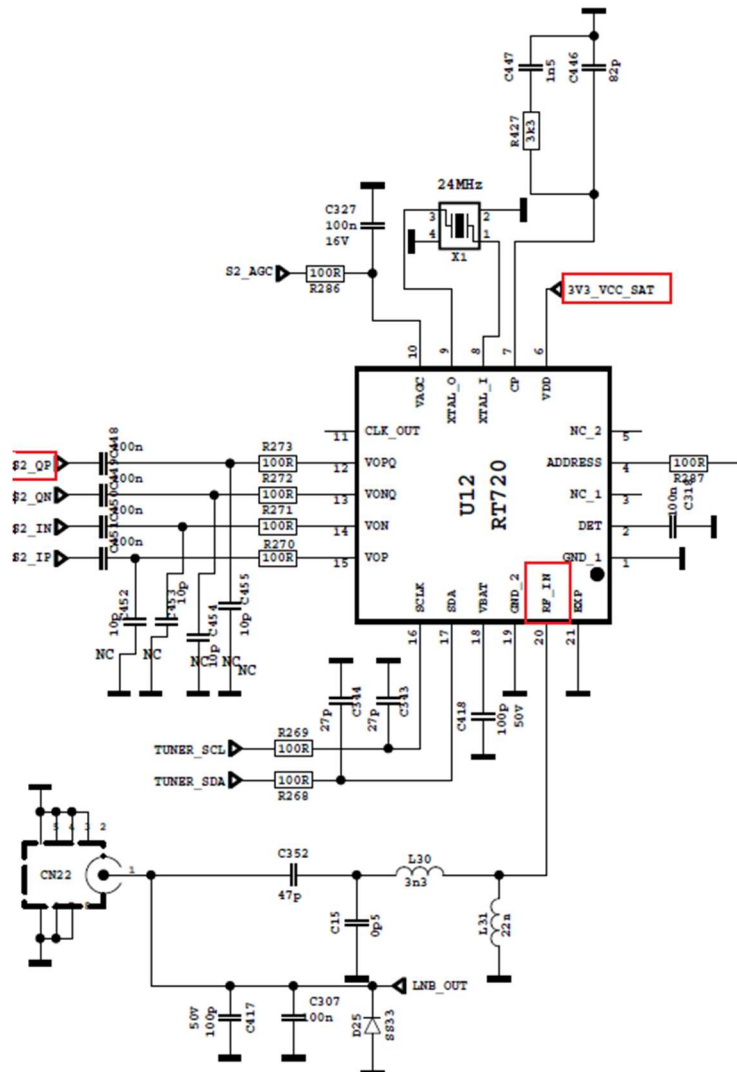
G. NO SIGNAL PROBLEM

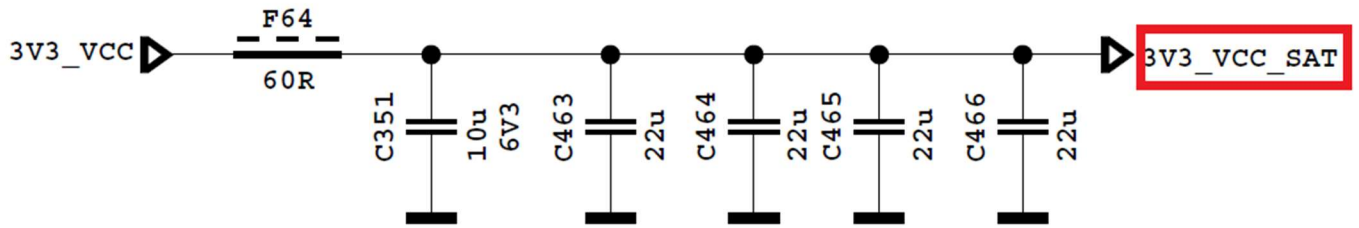
Problem: No signal or Low signal in DVB-S/S2 mode.

Check signal cables and LNB voltage, if there is no problem, check RT720 (U12) supply voltages; 3V3_VCC_SAT.

If the above measurements are OK, then measure the voltage from the PIN20 of U12.

If the PIN12 voltage is equal to 0V, please check i2c waveforms and software. If the PIN12 voltage is lower than 1V (e.g. 0.8V or 0.3V), change the U12 with a new part.





12. SERVICE MENU SETTINGS

In order to reach service menu, first Press “**MENU**” buton, then write “**4725**” by using remote controller. You can see the service menu main screen below. You can check SW releases by using this menu. In addition, you can make changes on video, audio etc. by using video settings, audio settings titles.



Figure 21: Service Menu

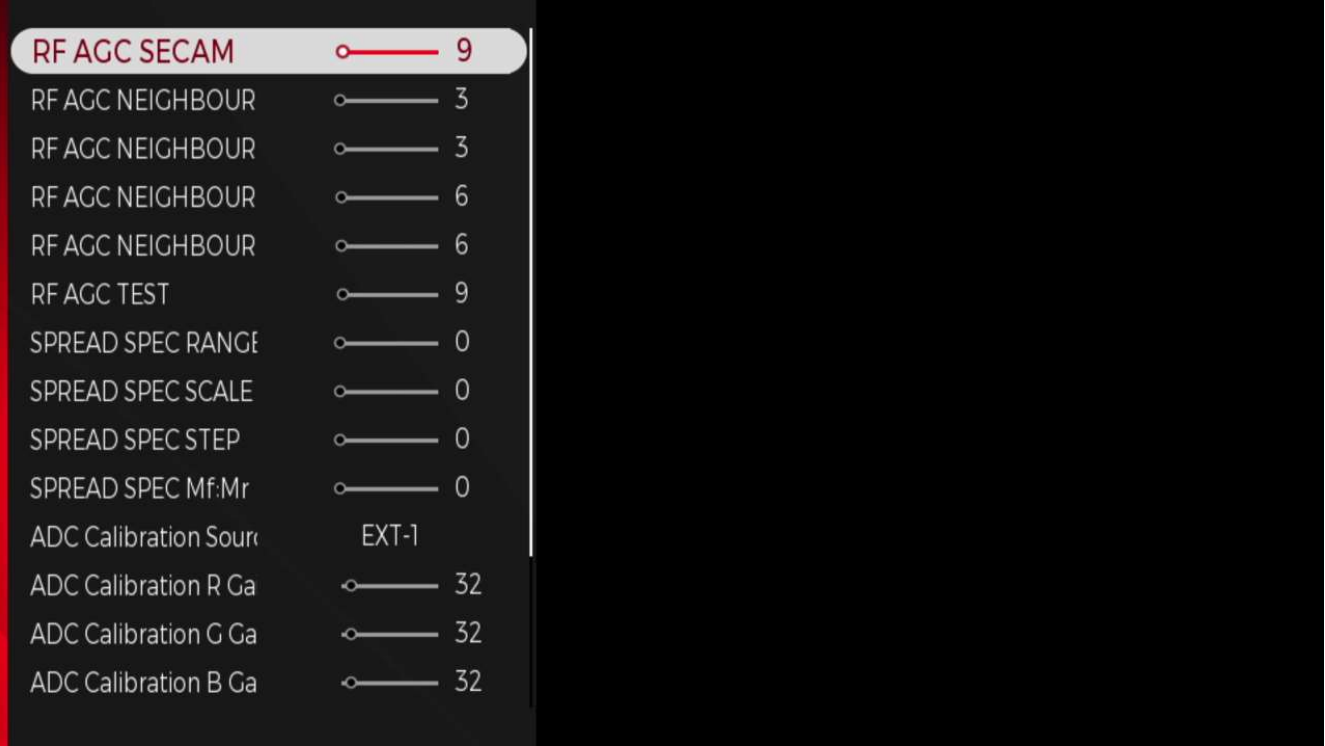


Figure 22: Video Settings

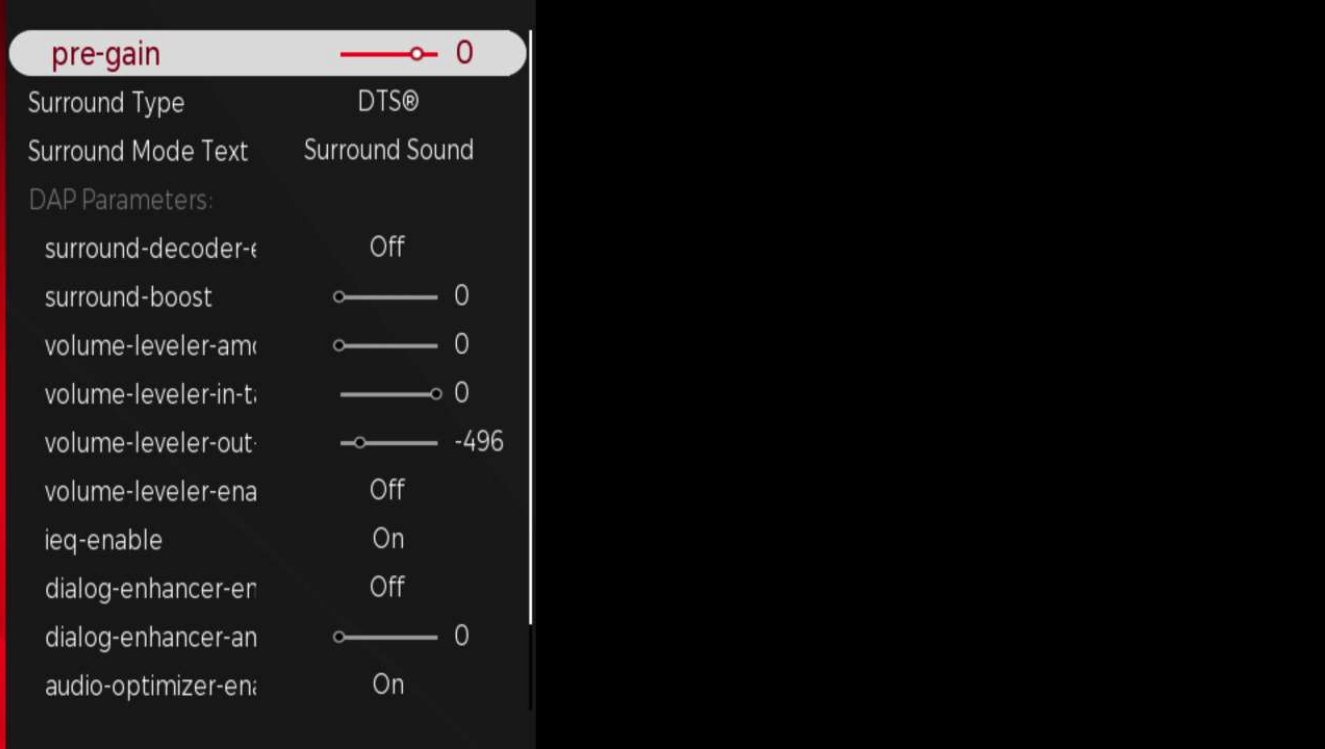


Figure 23: Audio Settings

Power Up Mode	Last State
Hotel Mode	Yes
Stby Search	Yes
Test Tool	Yes
Local Key	SingleTact
Volume Level	 24

Figure 24: Options 1

Aps Sorting	Disabled
Auto Zoom Mode	Disabled
EPG Menus	Enabled
Transparent Text	Disabled
HDMI Number	2
Rc Type	Rc45XX
DCF ID	6681.dcf
Touchpad Sw Versior	0
Video Wall ID	No

Figure 25: Options 2

HBBTV	Enabled
Portal	Vestel Portal
PVR	Enabled
Wifi	None
Customer	VESTEL
Cable Support	Yes
Satellite Support	Yes
DSmart	Disabled
Digiturk	Disabled
Orf	Disabled
Astra HD+	Enabled
Virtual Remote	Enabled
Follow Tv	Enabled
Open Browser	Enabled

Figure 26: Options 3

Tuner Type	R842
Tuner Firmware Versi	0x0
Tuner Build Number	0x0
Tuner T2 Demod FW	0x0

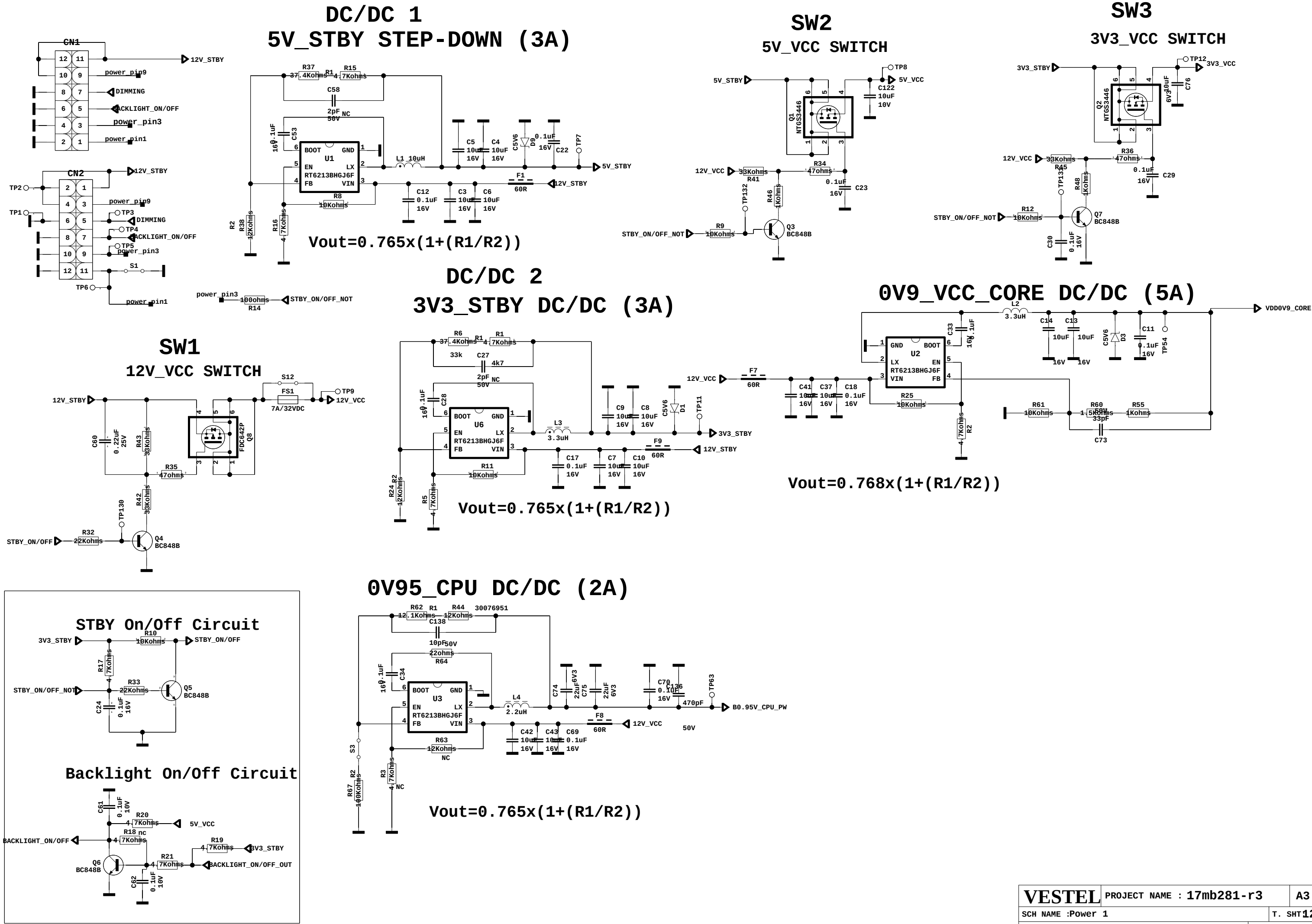
Figure 27: Tuning Settings

EXT1	No
EXT1 RGB	No
EXT1-S	No
EXT2	No
EXT2 RGB	No
EXT2-S	No
SIDE AV	No
S-VIDEO	No
HDMI1	Yes
HDMI2	Yes
HDMI3	No
HDMI4	No
YPbPr	Yes
VGA/PC	Yes

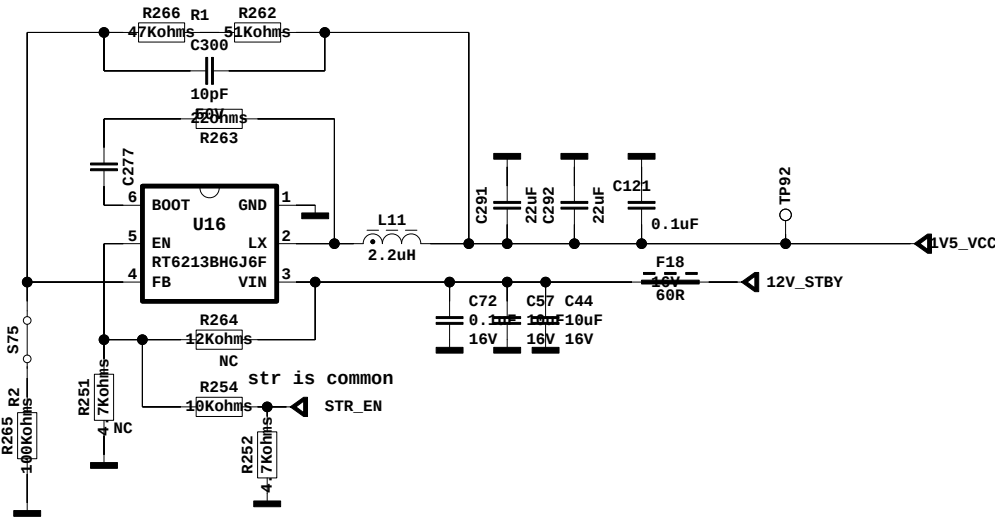
Figure 28: Source Settings

Remote control t	OK
Video Pattern Test	OK
UHF test	OK
VHF test	OK
Factory Reset	OK
Test mode service lis	
Tuner I2C	OK
IF I2C	OK
EDID status	OK
HDCP status	NOK
HDCP 2.X status	OK
WIDEVINE Status	NOK
DDR Settings	OK
CI+ credentials	NOK

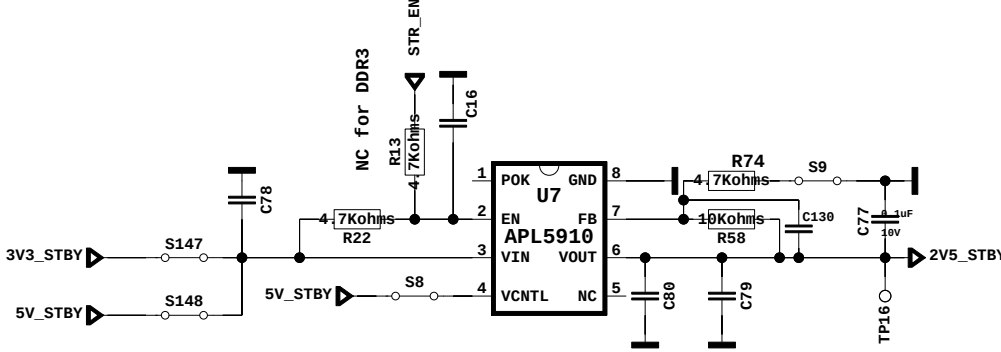
Figure 29: Diagnostic



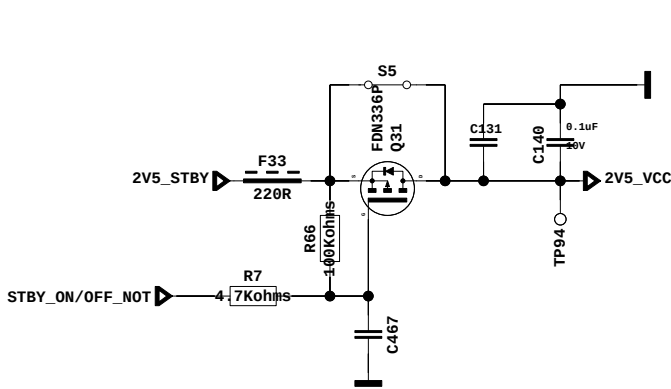
DC/DC 3
1V5_VCC DC/DC (2A)



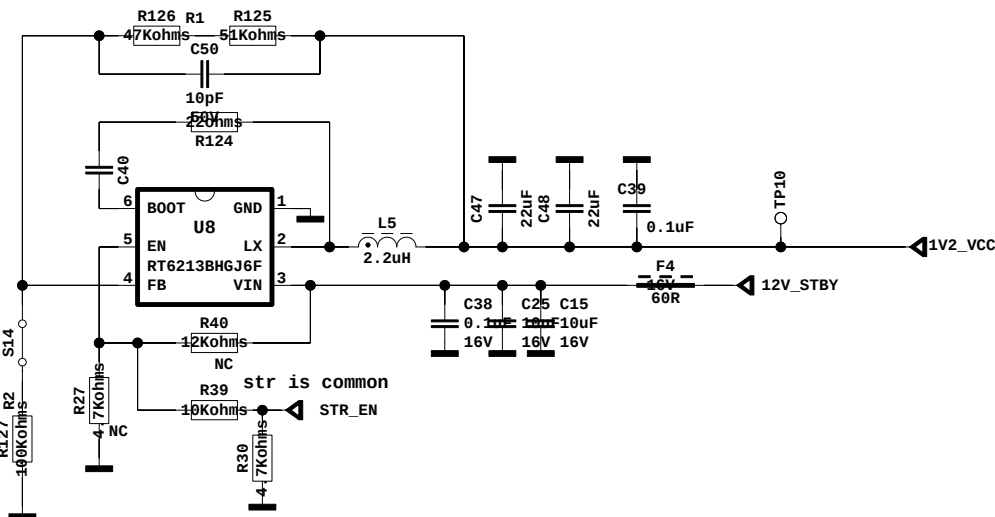
2V5_STBY LDO



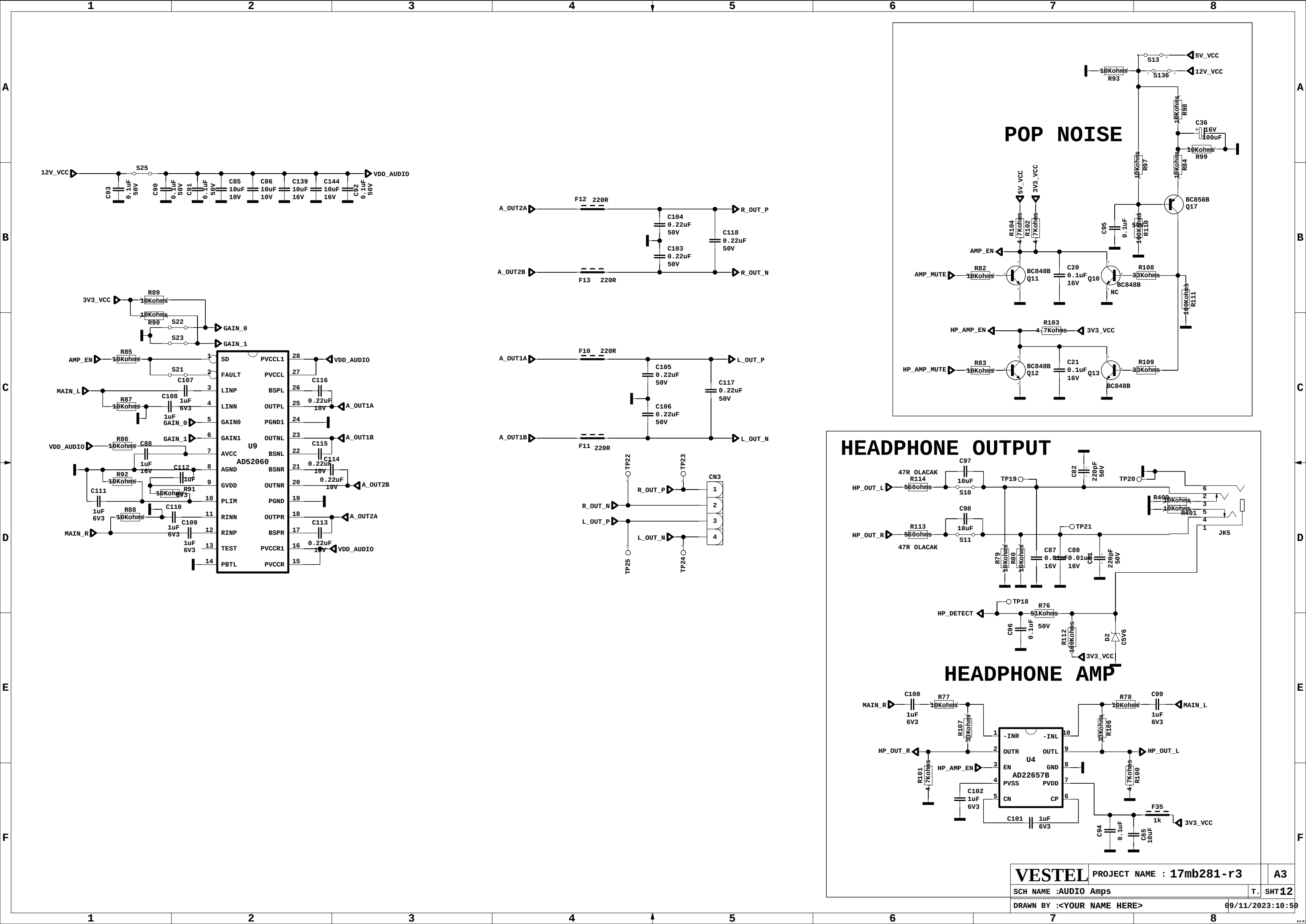
2V5_VCC_SW



1V2_VCC DC/DC (2A)



NC For DDR3



[illegible]