

A close-up photograph of a television circuit board. A large, dark integrated circuit (IC) is the central focus, with its numerous gold pins visible. To the left, a pink ribbon cable is connected to a multi-pin connector. Various electronic components are labeled with white text: 'U3' near the top left, 'C108' and 'C107' near the top left, 'C113' and 'C112' near the bottom left, and 'U5' near the bottom left. The board itself is a light blue color with intricate circuit traces.

MB181R IDTV

SERVICE MANUAL

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IMPORTANT

Before removing the rear cover from the TV for servicing, make sure that no cables are fixated to the cover. Release the cables from their clamps and disconnect (if any). Failure to do so may damage the wires and/or other components of the TV.

1. INTRODUCTION

17MB181R main board is driven by G36 MTK SOC. This IC is a single chip iDTV solution that supports channel decoding, MPEG decoding, and media-center functionality enabled by a high performance AV CODEC and CPU.

This board can be driven just 50Hz HD and FHD panels.

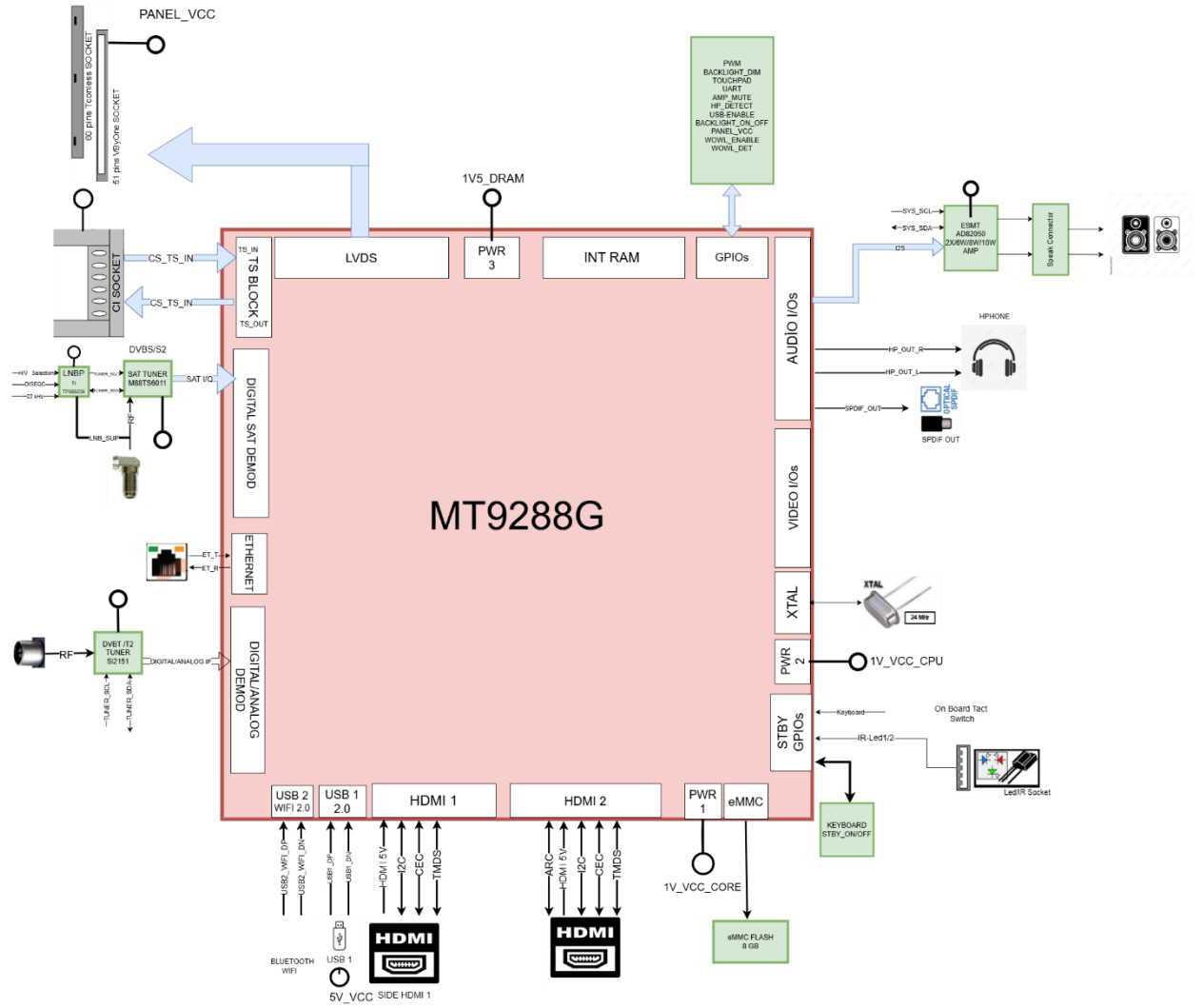
Key features include:

- Combo Front-End Demodulator
- A multi standart A/V format decoder
- The MACEpro video processor
- Home theatre sound processor
- Rich internet connectivity and completed digital home network solution
- Multi-purpose CPU for OS and multimedia
- Peripheral and power management
- Embedded DRAM (for connected option)

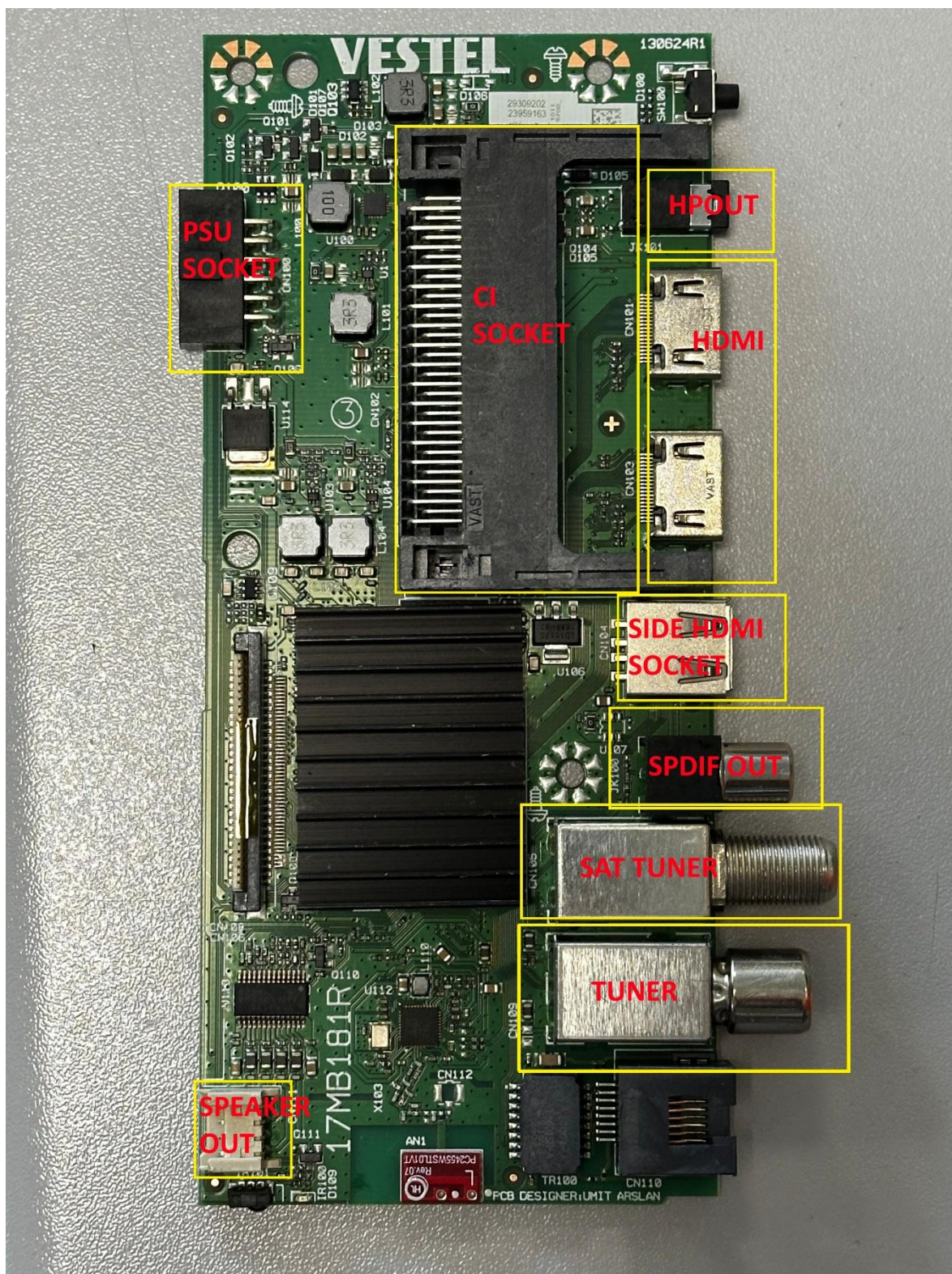
Supported peripherals are:

- 1 RF input VHF I, VHF III, UHF
- 1 Satellite input
- 1 Side AV (CVBS, R/L_Audio)
- 1xBack HDMI 1x Side HDMI input (with ARC option from 2nd input)
- 1 Common interface(Common)
- 1 Coax S/PDIF output
- 1 Headphone(Common)
- 1 USB(1X Side Common) and 1x internal USB for Wifi/Bluetooth
- 1 Ethernet-RJ45
- 1 Tact Switch

A. GENERAL BLOCK DIAGRAM



B. PLACEMENT OF BLOCKS



2. T/T2/C/A TUNER (U111)

Description

The Si2151 is Silicon Labs' sixth-generation hybrid TV tuner supporting all worldwide terrestrial and cable TV standards. Requiring no external balun, SAW filters, wirewound inductors or LNAs, the Si2151 offers the lowest-cost BOM for a hybrid TV tuner. Also included are an integrated power-on reset circuit and an option for single power supply operation. As with prior-generation Silicon Labs TV tuners, the Si2151 maintains very high linearity and low noise to deliver superior picture quality and a higher number of received stations when compared to other silicon tuners. The Si2151 offers increased immunity to WiFi and LTE interference, eliminating the need for external filtering. For the best performance with next-generation digital TV standards, such as DVB-T2/C2, the Si2151 delivers industry-leading phase noise performance.

Features

- Worldwide hybrid TV tuner
 - Analog TV: NTSC, PAL/SECAM
 - Digital TV: ATSC/QAM, DVBT2/T/C2/C, ISDB-T/C, DTMB
- 1.7 MHz, 6 MHz, 7 MHz, 8 MHz, and 10 MHz channel bandwidths
- 42-1002 MHz frequency range
- Industry-leading margin to A/74, NorDig, DTG, ARIB, EN55020, OpenCable™,DTMB
- Lowest BOM for a hybrid TV tuner
 - No balun, SAW filters, or external inductors required
 - Increased ESD protection on 4pins
- Best-in-class real-world reception
 - Lowest phase noise
 - High Wi-Fi and LTE immunity
- Low power consumption
 - 3.3 V and 1.8 V power supplies
 - Integrated 1.8 V LDO for 3.3 V singlesupply operation
- Integrated power-on reset circuit
- Standard CMOS process
- 3x3 mm, 24-pin QFN package
- RoHS compliant

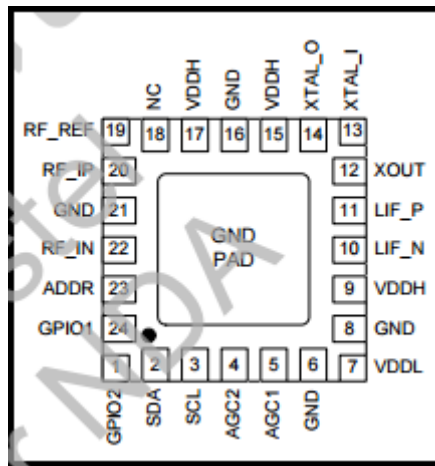


Figure 1: Si2151 Pin description

Pin Number(s)	Name	I/O	Description
1*	GPIO2	I/O	General purpose input/output #1
2	SDA	I/O	I ² C data input/output
3	SCL	I	I ² C clock input
4*	AGC2	I	LIF output amplitude control input #2
5*	AGC1	I	LIF output amplitude control input #1
6	GND	S	Ground
7	VDDL	S	Low supply voltage, 1.8 V (leave caps connected for single supply case)
8	GND	S	Ground
9	VDDH	S	High supply voltage, 3.3 V
10	LIF_N	O	Negative LIF differential output to SoC or DTV/ATV demodulator
11*	LIF_P	O	Positive LIF differential output to SoC or DTV/ATV demodulator
12	XOUT	O	Output reference clock to secondary tuner or receiver
13	XTAL_I	I	Crystal pin 1 (or RCLK input driven by XOUT of another tuner or receiver)
14	XTAL_O	O	Crystal pin 2 (leave floating if XTAL_I is driven by XOUT of another tuner or receiver)
15	VDDH	S	High supply voltage, 3.3 V
16	GND	S	Ground

17	VDDH	S	High supply voltage, 3.3 V
18*	NC	NC	No connect
19	RF_REF	O	RF reference voltage output
20	RF_IP	I	RF input (positive)
21	GND	S	Ground
22	RF_IN	I	RF input (negative)
23	ADDR	I	I ² C address select
24*	GPIO1	I/O	General purpose input/output #1
*Note: Pin should be left floating if unused.			

Table 1: Si2151 Pin function

3. S/S2 TUNER (U110) OPTIONAL

Description

M88TS6011 is a single chip, direct-conversion tuner for digital satellite receiver applications. Its offers the industry's most integrated solution to a satellite tuner function, simplifying the front-end design. This device incorporates the following function blocks on a single chip: an LNA, quadrature down-converting mixers, a low phase noise and fast locking frequency synthesizer with on-chip loop filters, a DC offset cancellation loop with integrated loop filters, self-calibrated programmable baseband channel filters, an integrated RF AGC loop, and crystal oscillators with and integrated auxiliary clock output.

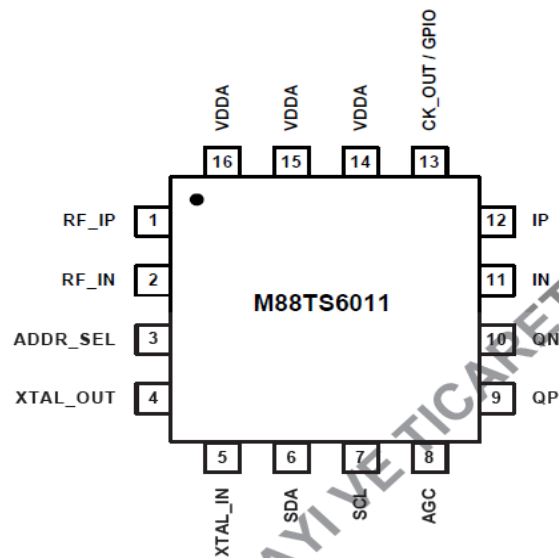
As a result of integrating all these blocks, the M88TS6011 has the least number of pins compared with other conventional solutions, and requires the least external compopnents. In typical applications, M88TS6011 requires only one crystal, one matching network, and a few external capacitors. The device also has the industry's smallest latency, as it uses a fast locking PLL and fast settling DC offset cancellation architecture.

The M88TS6011 can be configured via a 2-wire serial bus. The chip is available in a 16-pin QFN package.

Features

- Single-Chip tuner
- Compliant with DVB-S2 and ABS-S standards
- Support QPSK, 8PSK, 16APSK AND 32APSK
- Direct-conversion from L-band to baseband
- Symbol rate:1 to 45 Msybol/s
- Integrated VCOs and PLL, with on-chip inductors varactors and loop filter
- Integrated baseband filters: 6 MHz to 40 MHz bandwith
- Integrated RF AGC for optimal performance
- Integrated baseband DC offset cancellation removes external loop filters
- Excellent immunity to strong adjacent undersired channels
- Integrated clock driver provides auxiliary divided clock output for other devices
- Support sleep mode
- 2-wire serial bus with 3.3V compatible logic levels

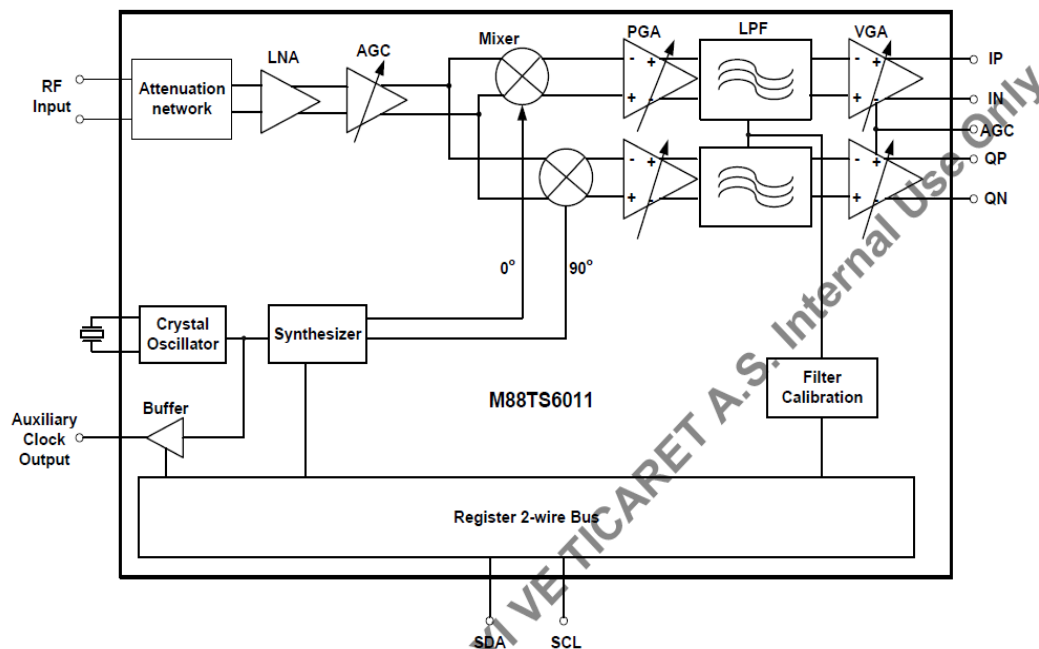
- Power supply: +3.3V
- Package: 16-pin E-PAD QFN
- RoHS compliant



Ground – The exposed pad at the bottom of the package.

Figure 2: Pin description

Block Diagram



4. AUDIO AMPLIFIER STAGES

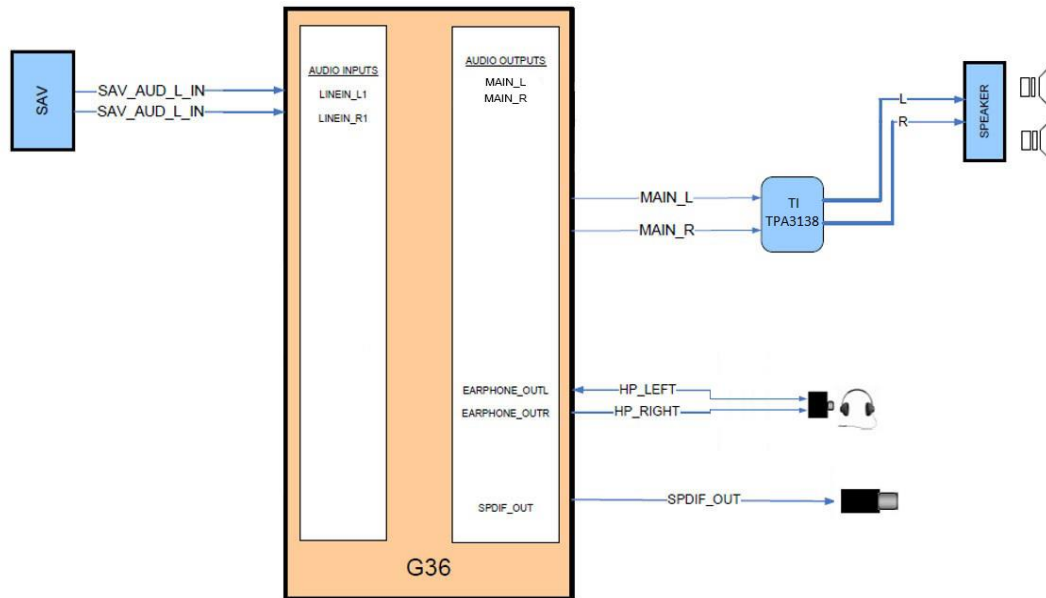


Figure 3: The block diagram of the audio part

A. MAIN AMPLIFIER (U137) (10-W)

Description

The TPA3138D2 is a 10-W/ch, high-efficiency, lowidle- current Class-D stereo audio amplifier. It can drive stereo speakers with a load as low as 3.2-Ω. In the 1SPW mode, it consumes a low idle current of only 21-mA (12-V) and can operate down to 3.5-V, allowing for longer audio play and improved thermal performance in bluetooth speakers, battery-powered appliances and other power-sensitive applications.

Advanced EMI Suppression with Spread Spectrum Control enables the use of inexpensive ferrite bead filters while meeting EMC requirements for system cost reduction.

To further simplify the design, the TPA3138D2 integrates essential protection features including undervoltage, overvoltage, power limit, short circuit, overtemperature, as well as DC speaker protection. All of these protections come with automatic recovery.

Features

- Wide Supply Range 3.5-V to 14.4-V
 - 2 × 10 W into 6-Ω, 1% THD+N, 12-V Supply
 - 1 x 18.5 W into 4-Ω, 10% THD+N, 12-V Supply
 - THD+N : 0.04% at 1 W, 1 kHz input, 6-Ω
- Longer Battery Life for Portable Applications:
 - 20-mA (12-V) Idle Current in 1SPW Mode
 - >90% Class-D Efficiency
- Reduced Solution Size and Cost:
 - Inductor-Free Operation

- EN55013 and EN55022 EMC Compliant When No Inductors are Used
- No External Heatsink Required
- Flexible Audio Solution:
 - Single-ended or Differential Analog Inputs
 - Selectable Gain: 20 dB and 26 dB
 - Pop and Click-Free Startup
- Integrated Protections and Auto Recovery:
 - Pin-to-pin, Pin-to-Ground, and Pin-to-Power Short Circuit Protection
 - Thermal Protection, Undervoltage Protection, and Overvoltage Protection
 - Power Limiter and DC Speaker Protection
- Pin-to-Pin Compatible with TPA3110D2, TPA3136D2 and TPA3136AD2

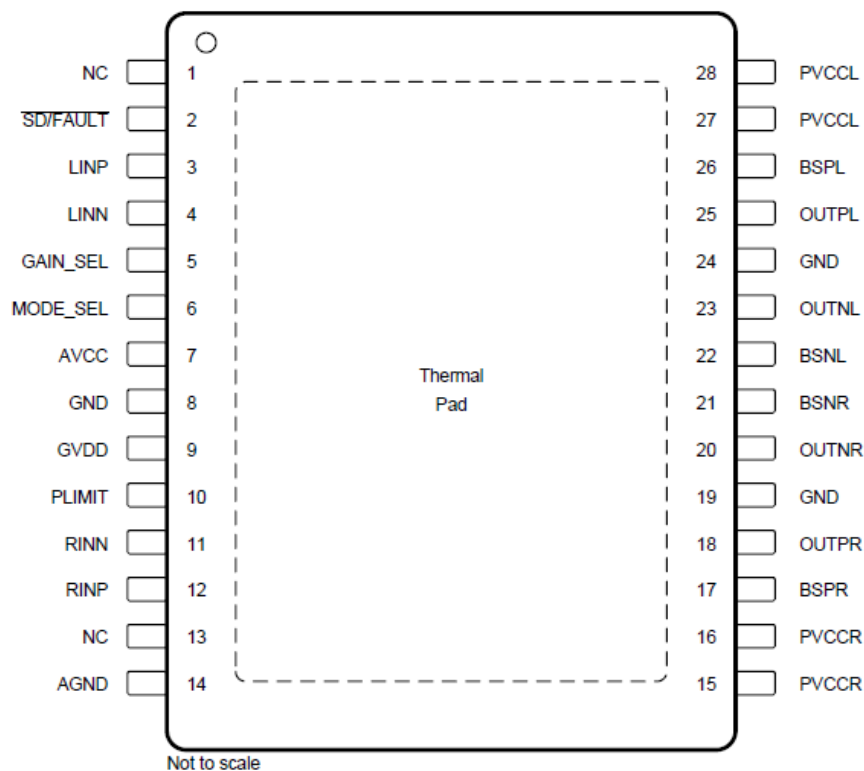


Figure 4: Pin description

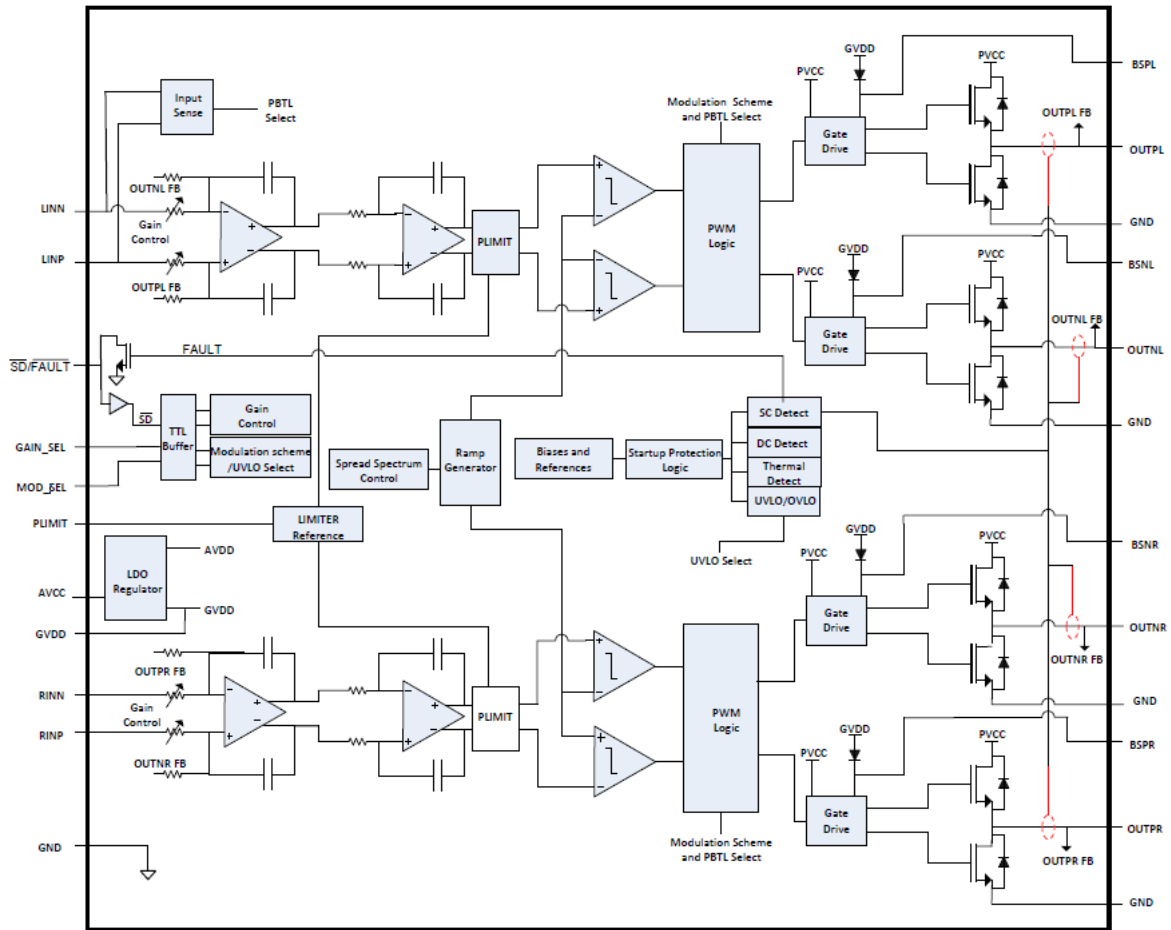


Figure 5: Functional Block Diagram

		MIN	MAX	UNIT
Supply voltage	AVCC to GND, PVCC to GND	-0.3	20	V
Input current	To any pin except supply pins		10	mA
Interface pin voltage	$\overline{\text{SD/FAULT}}$ to GND ⁽²⁾ , GAIN_SEL, MODE_SEL	-0.3	AVCC + 0.3	V
			10	V/ms
	PLIMIT	-0.3	GVDD + 0.3	V
	RINN, RINP, LINN, LINP	-0.3	5.5	V
Minimum load resistance, R_L	BTL, (10 V < PVCC < 14.4 V)	4.8		Ω
	BTL, (3.5 V < PVCC < 10 V)	3.2		
	PBTL, (10 V < PVCC < 14.4 V)	2.4		
	PBTL, (3.5 V < PVCC < 10 V)	1.6		
Continuous total power dissipation		See the Thermal Information Table		
Operating Junction Temperature range		-25	150	°C
Storage temperature range, T_{stg}		-40	125	°C

Table 2: Absolute Maximum Ratings

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V _{CC}	Supply voltage	PVCC, AVCC	3.5	14.4	V
V _{IH}	High-level input voltage	$\overline{SD/FAULT}^{(1)}$, GAIN_SEL, MODE_SEL	2	AVCC	V
V _{IL}	Low-level input voltage	$\overline{SD/FAULT}$, GAIN_SEL, MODE_SEL ⁽²⁾		0.8	V
V _{OL}	Low-level output voltage	$\overline{SD/FAULT}$, R _{PULL-UP} = 100 k Ω , PVCC = 14.4 V		0.8	V
I _{IH}	High-level input current	$\overline{SD/FAULT}$, GAIN_SEL, MODE_SEL, V _I = 2 V, AVCC = 12 V		50	μ A
I _{IL}	Low-level input current	$\overline{SD/FAULT}$, GAIN_SEL, MODE_SEL, V _I = 0.8 V, AVCC = 12 V		5	μ A
T _A	Operating free-air temperature ⁽³⁾		-10	85	°C
T _J	Operating junction temperature ⁽³⁾		-10	150	°C

Table 3: Recommended Operating Conditions

5. POWER STAGE

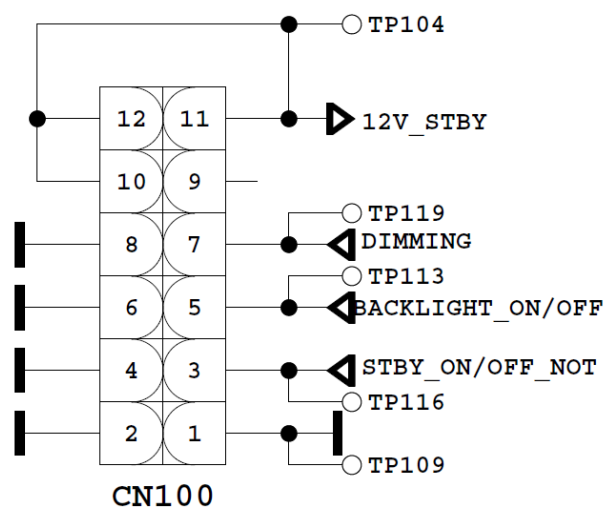


Figure 6: Power Socket and Power Options

Power socket is used for taking voltage which is 12V_STBY . These voltages are produced in power card. Also socket is used for giving dimming, backlight and standby signals with power card. Power socket pinning is shown in above figure.

12V_STBY is converted several different voltages on the mainboard which are shown in below figure.

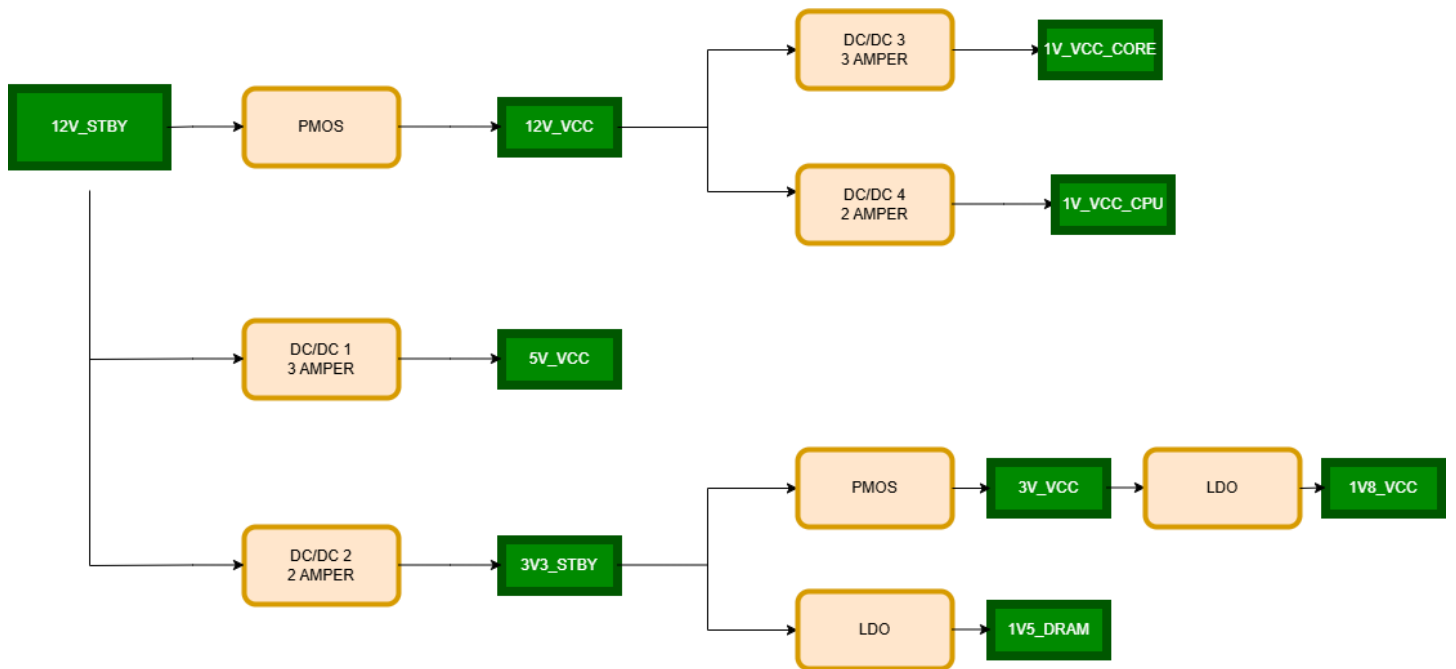


Figure 7: Power Block Diagram

List of the components:

- PMOS(Q103,Q100) → KI5P02DV
- DC-DC-1(U101) → TPS563203
- DC-DC-2(U102) → TPS563203-3A
- DC-DC-3(U104) → TPS563203-3A
- DC-DC-4(U103) → TPS563203-2A
- LDO(U106,U114) → LM1117

A. KI5P02DV (Q100,Q103)

Features

- VDS (V) = -20V
- ID = -4.6 A
- RDS(ON) < 40mΩ (VGS = -4.5V)
- RDS(ON) < 70mΩ (VGS = -2.5V)
- Low Input/Output Leakage

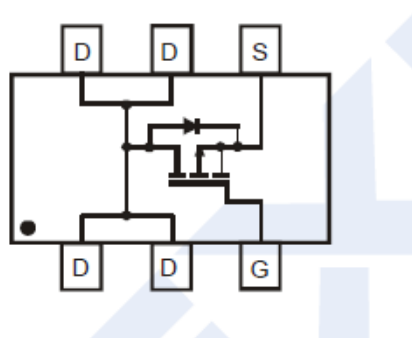


Figure 8: Pin description

■ Electrical Characteristics Ta = 25°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V _{DSS}	I _D =-250 μ A, V _{GS} =0V	-20			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-20V, V _{GS} =0V			-1	μ A
Gate-Body leakage current	I _{GSS}	V _{DS} =0V, V _{GS} = $\pm$ 12V			$\pm$ 100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250 μ A	-0.6		-1.2	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =-4.5V, I _D =-4.6A			40	m Ω
		V _{GS} =-2.5V, I _D =-3.8A			70	
On state drain current	I _{D(ON)}	V _{GS} =-4.5V, V _{DS} =-5V	-15			A
Forward Transconductance	g _{FS}	V _{DS} =-10V, I _D =-4.6A		9		S
Input Capacitance	C _{iss}	V _{GS} =0V, V _{DS} =-15V, f=1MHz		820		pF
Output Capacitance	C _{oss}			200		
Reverse Transfer Capacitance	C _{rss}			160		
Gate resistance	R _g	V _{GS} =0V, V _{DS} =0V, f=1MHz		2.5		Ω
Total Gate Charge	Q _g	V _{GS} =-4.5V, V _{DS} =-10V, I _D =-4.5A		10.1		nC
Gate Source Charge	Q _{gs}			1.5		
Gate Drain Charge	Q _{gd}			4.3		
Turn-On DelayTime	t _{d(on)}	V _{DS} = -10V, V _{GS} = -4.5V, I _D = -1A, R _G = 6 Ω		4.4		ns
Turn-On Rise Time	t _r			9.9		
Turn-Off DelayTime	t _{d(off)}			28		
Turn-Off Fall Time	t _f			23.4		
Maximum Body-Diode Continuous Current	I _S				-1.7	A
Diode Forward Voltage	V _{SD}	I _S =-2.1A, V _{GS} =0V	-0.5		-1.4	V

Figure 9: Electrical Characteristic

B. TPS563203(U101,U102,U103,U104)

3 Description

TPS563203, TPS563206 is a simple, easy-to-use, 3-A synchronous buck converter in a SOT563 package.

The device is optimized to operate with minimum external component counts and also optimized to achieve low standby current.

This switch mode power supply (SMPS) device employs D-CAP3 control mode providing a fast transient response and supporting both low-equivalent series resistance (ESR) output capacitors such as specialty polymer and ultra-low ESR ceramic capacitors with no external compensation components.

TPS563203 operates in ECO mode, which maintains high efficiency during light load operation. TPS563206 operates in FCCM mode, which keeps the same frequency and lower output ripple during all load conditions. It integrates complete protection through OCP, UVLO, OTP, and UVP with hiccup. TPS56320x is available in a 6-pin 1.6-mm $\times$ 1.6-mm SOT563 (DRL) package, and specified from a -40°C to 125°C junction temperature.

1 Features

- Configured for a wide range of applications
 - Input voltage range: 4.2 V to 17 V
 - Output voltage range: 0.6 V to 7 V
 - Reference voltage: 0.6 V
 - $\pm 1.5\%$ reference voltage accuracy at 25 °C
 - $\pm 2\%$ reference voltage accuracy at -40°C to 125°C
 - Integrated 110-m Ω and 60-m Ω FETs
 - Low quiescent current for TPS563203: 110 μA
 - Switching frequency: 600 kHz
 - Maximum 95% large duty cycle operation
 - Fixed soft-start time: 1.4 ms
- Easy of use and small solution size
 - ECO mode (TPS563203) and FCCM mode (TPS563206) at light loading
 - D-CAP3™ control mode with fast transient response
 - Support start-up with prebiased output
 - Non-latch for OV, OT, and UVLO protection
 - Cycle-by-cycle over current limit
 - Hiccup mode for UV protection
 - Operating junction temperature range from -40°C to 125°C
 - SOT563 package 1.6 mm $\times$ 1.6 mm

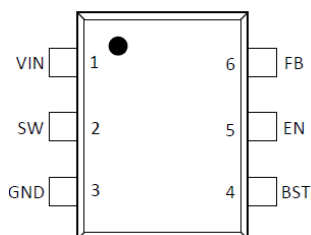


Figure 10: Pin Assignment

PIN		I/O	DESCRIPTION
NAME	NO.		
VIN	1	I	Input voltage supply pin
SW	2	O	Switch node connection between high-side NFET and low-side NFET
GND	3	—	Ground pin Source terminal of low-side power NFET as well as the ground terminal for controller circuit. Connect sensitive FB to this GND at a single point.
BST	4	O	Supply input for the high-side NFET gate drive circuit. Connect a 0.1- μF capacitor between the BST and SW pin.
EN	5	I	Enable input control. Active high and must be pulled up to enable the device.
FB	6	I	Converter feedback input. Connect to output voltage with feedback resistor divider.

6.5 Electrical Characteristics

Over operating $T_J = -40^{\circ}\text{C} - 125^{\circ}\text{C}$, $V_{\text{VIN}} = 12\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY VOLTAGE						
VIN	Input voltage range	VIN	4.2		17	V
I _{VIN}	VIN Supply Current	No load, $V_{\text{EN}} = 5\text{ V}$, non-switching, PSM version		110		μA
		No load, $V_{\text{EN}} = 5\text{ V}$, $V_{\text{FB}} = 0.7\text{ V}$, FCCM version		350		μA
I _{INSDN}	VIN Shutdown Current	No load, $V_{\text{EN}} = 0\text{ V}$		7		μA
UVLO						
UVLO	VIN Undervoltage Lockout	Wake up VIN voltage	3.6	3.8	4	V
UVLO	VIN Undervoltage Lockout	Shut down VIN voltage	3.2	3.4	3.6	V
UVLO	VIN Undervoltage Lockout	Hysteresis VIN voltage		400		mV
FEEDBACK VOLTAGE						
VFB	FB voltage	$T_J = 25^{\circ}\text{C}$, $V_{\text{in}} = 4.2 - 17\text{ V}$	591	600	609	mV
VFB	FB voltage	$T_J = -40^{\circ}\text{C}$ to 125°C , $V_{\text{in}} = 4.2 - 17\text{ V}$	588	600	612	mV
MOSFET						
R _{DS(ON)HI}	High-side MOSFET R _{ds(on)}	$T_J = 25^{\circ}\text{C}$, $V_{\text{VIN}} \geq 5\text{ V}$		110		m Ω
R _{DS(ON)LO}	Low-side MOSFET R _{ds(on)}	$T_J = 25^{\circ}\text{C}$, $V_{\text{VIN}} \geq 5\text{ V}$		60		m Ω
DUTY CYCLE and FREQUENCY CONTROL						
F _{SW}	Switching Frequency (1)	$T_J = 25^{\circ}\text{C}$, $V_{\text{VOUT}} = 1.0\text{ V}$		600		kHz
T _{OFF(MIN)}	Minimum Off-time	$V_{\text{FB}} = 0.5\text{ V}$		100		ns
T _{ON(MIN)}	Minimum On-time	$T_J = 25^{\circ}\text{C}$		55		ns
CURRENT LIMIT						
I _{OCL_LS}	Over Current threshold	Valley current set point	3	3.9	4.7	A
I _{NOCL}	Negative Over Current threshold	Valley current set point	1	1.8	2.5	A
LOGIC THRESHOLD						
V _{EN(ON)}	EN Threshold High-level	$V_{\text{in}} = 4.2 - 17\text{ V}$	1.15	1.2	1.28	V
V _{EN(OFF)}	EN Threshold Low-level	$V_{\text{in}} = 4.2 - 17\text{ V}$	0.93	1	1.05	V
V _{ENHYS}	EN Hysteresis			200		mV
OUTPUT DISCHARGE and SOFT START						
I _{EN}	EN Pull down current	$V_{\text{EN}} = 1.5\text{ V}$		1		μA
t _{SS}	Internal Soft-start Time			1.4		ms

Table 4: Functional Pin Description & Electrical Characteristics

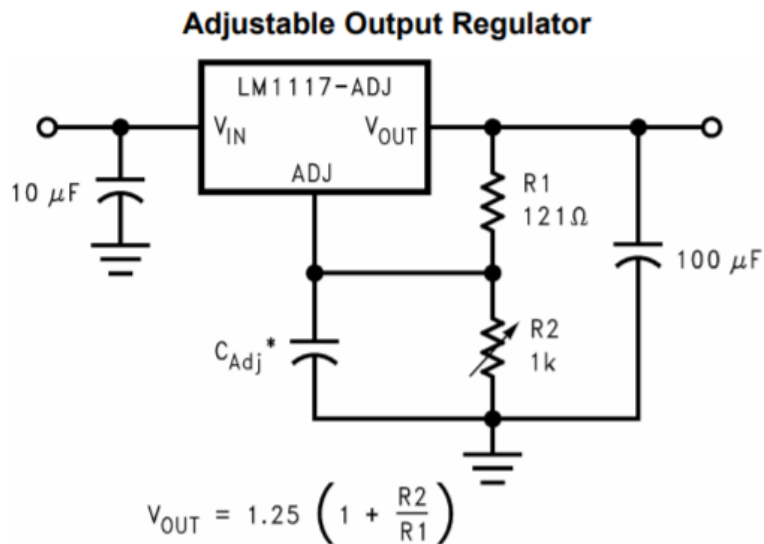
C. LM1117 (U114,106)

General Description

The LM1117 is a low dropout voltage regulator with a dropout of 1.2 V at 800 mA of load current. The LM1117 is available in an adjustable version which can set the output voltage from 1.25 to 13.8 V with only two external resistors. In addition, it is available in five fixed voltages, 1.8 V, 2.5 V, 3.3 V, and 5 V. The LM1117 offers current limiting and thermal shutdown. Its circuit includes a Zener trimmed bandgap reference to assure output voltage accuracy to within $\pm 1\%$. A minimum of 10- μF tantalum capacitor is required at the output to improve the transient response and stability.

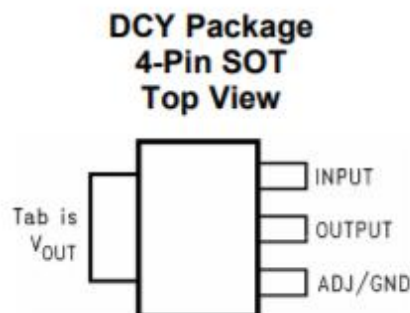
Features

- Available in 1.8 V, 2.5 V, 3.3 V, 5 V, and Adjustable Versions
- Space-Saving SOT-223 and WSON Packages
- Current Limiting and Thermal Protection
- Output Current 800 mA
- Line Regulation 0.2% (Maximum)
- Load Regulation 0.4% (Maximum)
- Temperature Range
 - LM1117: 0°C to 125°C
 - LM1117I: -40°C to 125°C



* C_{Adj} is optional, however it will improve ripple rejection.

Pin Configuration and Functions



Pin Functions

NAME	PIN					I/O	DESCRIPTION
	TO-252	WSON	SOT-223	TO-263	TO-220		
ADJ/GND	1	1	1	1	1	—	Adjust pin for adjustable output option. Ground pin for fixed output option.
V _{IN}	3	2, 3, 4	3	3	3	I	Input voltage pin for the regulator
V _{OUT}	2, TAB	5, 6, 7, TAB	2, 4	2, TAB	2, TAB	O	Output voltage pin for the regulator

Table 5: Functional Pin Description

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	MIN	MAX	UNIT
Maximum Input Voltage (V _{IN} to GND)		20	V
Power Dissipation ⁽²⁾	Internally Limited		
Junction Temperature (T _J) ⁽²⁾		150	°C
Lead Temperature	TO-220 (T) Package, 10 s		260
	SOT-223 (MP) Package, 4 s		260
Storage Temperature, T _{stg}	–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The maximum power dissipation is a function of T_{J(max)}, R_{θJA}, and T_A. The maximum allowable power dissipation at any ambient temperature is P_D = (T_{J(max)} – T_A)/R_{θJA}. All numbers apply for packages soldered directly into a PCB.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Input Voltage (V _{IN} to GND)		15	V
Junction Temperature (T _J) ⁽¹⁾	LM1117	0	125
	LM1117I	–40	125

- (1) The maximum power dissipation is a function of T_{J(max)}, R_{θJA}, and T_A. The maximum allowable power dissipation at any ambient temperature is P_D = (T_{J(max)} – T_A)/R_{θJA}. All numbers apply for packages soldered directly into a PCB.

6. MICROCONTROLLER

MEDIATEK G36 (U109)

The MT9288Gxxxxx is MediaTek's latest SOC solution for FHD smart TV. Based on MediaTek's advanced technologies, the MT9288Gxxxxx is integrated with the high-quality video processor which satisfies a variety of customer's requests for image quality to develop the state-of-the-art DTV system. The multi-core CPUs and GPUs deliver high performance for modern Linux and Android TVs. The up-to-date ARM and Mali architecture ensures the best software compatibility.

Applications, such as HTML5, Java, Flash, and so on, are implemented with less efforts.

The MediaTek Professional PQ Engine includes all of MediaTek's most advanced color-tuning tools. MediaTek unique color processor with specially-designed color remapping systems assist System-developers to identify PQ characteristics of all the range of panel models quickly and easily.

The MT9288Gxxxxx for DTV/MM/OTT applications into a single device, reducing the overall system BOM cost. With versatile peripheral connectivity ports, like HDMI, USB, Ethernet, CVBS, etc., the MT9288Gxxxxx can serve as a highquality media center in home entertainment field.

To meet the increasingly popular energy legislative requirements without the use of additional hardware, the MT9288Gxxxxx has an ultra-low power standby mode during which an embedded MCU can act upon standby events and wake up the system as required.

MT9288Gxxxxx is a highly integrated smart TV solution, which supports LVDS output, DTV channel decoding, MPEG decoding, AV1 decoding, and security OS. MT9288Gxxxxx serves full functions of multi-media centers with a high performance CPU, GPU, and AV CODEC/security engines.

1. Combo Front-End Demodulators
2. Advanced Multi-Core CPU and 3D GPU
3. 3D Formatter Engine
4. Multi-Standard A/V Format Decoder
5. MediaTek High Performance Video Processor and MediaTek Professional PQ Engine
6. Home Theater Sound Processor
7. Internet and Variety of Connectivity Support
8. Peripheral and Power Management
9. Robust and Efficient Security Engine
10. Full Multi-Media Decoders Including AV1/HEVC Decoder Supporting up to FHD/60fps Resolution

High Performance Micro-processor

- ARM Advanced Multi-Core Cortex CPU
- 32KB/32KB I/D cache
- 512KB L2 cache
- Supports Neon instruction sets

3D Graphic GPU

- ARM Advanced Multi-Core Mali GPU
- Vulkan 1.1
- Supports OpenGL ES 3.2/2.0/1.1
- Supports OpenCL 2.0
- Supports DirectX 11 FL9_3
- Supports rendering size up to FHD

Transport Stream De-multiplexer

Supports two parallel and one serial TS inputs interfaces, with or without sync signal

- Supports one of TS PAD is programmable TS
- input/output
- Supports external demodulators

- TS data rate is 140Mbit/s for serial and
- 56MByte/s for parallel
- 128 general purpose PID filters and 128
- section filters for all transport stream demultiplexer
- Supports additional audio/video/PCR filters
- Supports time-shift
- Supports 3DES/DES and AES encryption/decryption
- Supports dual stream decoding for 3D content

MPEG-2 Video Decoder

- ISO/IEC 11172-2 MPEG-1 video format
- decoding
- ISO/IEC 13818-2 MPEG-2 video MP@HL and
- HD level
- Supports resolution up to HDTV (1080p60, 1080i, 720p) and SDTV
- Supports dual stream decoding for 3D content

MPEG-4 Video Decoder

- ISO/IEC 14496-2 MPEG-4 ASP video decoding
- up to HD level
- Supports resolutions up to HDTV (1080p@60fps)
- Supports Divx Home Theater & HD profiles
- Supports FLV version1 video format decoding

H.264 Decoder

ITU-T H.264, ISO/IEC 14496-10 (main and high profile up to level 4.2) video decoding

Supports resolution up to 1920x1080@60fps
Supports bitrate up to 62.5Mbps, the upper limit of level 4.2

Advanced sound processing options available, for example: Dolby1, DTS2, DBX-TV3

Supports digital audio format :
MPEG-1, MPEG-2 (Layer I/II), MP3, AAC-LC, HE-AAC, WMA, WMA9 Pro

Supports Multi-stream programs :
Dolby MS12-B **Optional**, Dolby MS12-D **Optional**,

Dolby MS12-Y **Optional**, Dolby MS12-Z **Optional**, and

DTS M6 **Optional**, DTS M6 multistream decoder/encoder

Supports Audio Description

Supports MPEG audio encoding

Supports time-shifting PVR

Supports programmable delay for audio/video Synchronization

Audio Interface

- One L/R audio line-input
- One L/R output for main speaker or additional line-output
- Supports stereo headphone driver
- I2S digital audio output
- S/PDIF digital audio output and input **optional**
- Supports HDMI receiver ARC function
- Supports PDM input for 2/4 channels digital
- Microphone

Analog RGB Compliant Input Ports

- One analog ports support up to 1080P
- Supports PC RGB input up to SXGA@75Hz
- Supports HDTV RGB/YPbPr/YCbCr
- Supports Composite Sync and SOG Sync-on-Green
- Automatic color calibration

Analog RGB Auto-Configuration & Detection

- Auto input signal format and mode detection
- Auto-tuning function including phasing, positioning, offset and gain configuration
- Sync Detection for H/V Sync

DVI/HDCP/HDMI Compliant Input Ports

- Three HDMI/DVI input ports
- HDMI 1.4b Compliant
- MediaTek iSwitch for fast HDMI switching
- HDCP 2.2/1.4 Compliant
- Supports HDMI CEC
- Supports HDMI ARC TX
- Robust receiver with excellent long-cable support

MediaTek High Performance Video Processor

- Video Processing Engine
 - Supports up to 2K FHD@60p
 - 10/12-bit Internal Data Processing
 - Arbitrary Frame Rate Conversion
- Video Care Technology
 - Video Line Broken Artifact Detection and Removal
 - Video Detection & Repairing Technology for Lousy Inputs such as Internet Streaming
- Fully Programmable Multi-Function Scaling Engine
 - High-Quality Filters with Programmable Parameter
 - An advanced Zoom Algorithm providing Aliasing/Ringing Suppression
 - Nonlinear Video Scaling supports various modes including Panorama
 - Supports Dynamic Scaling for RM, VC-1
 - Fully Programmable Zoom Ratios for Up/Down Scaling
 - Independent Horizontal and Vertical Zoom
- Deinterlacer
 - Motion Compensated Video Deinterlacing with Motion Object Stabilizer
 - Motion Adaptive Deinterlacer
 - Edge-Oriented Deinterlacer with Edge Smoothing and Artifact Removal
 - Automatic 3:2:2/M:N Pull-Down
- Advanced sound processing options available, for example: Dolby1, DTS2, DBX-TV3
- Supports digital audio format :
MPEG-1, MPEG-2 (Layer I/II), MP3, AAC-LC, HE-AAC, WMA, WMA9 Pro

- Supports Multi-stream programs :
Dolby MS12-B **Optional**, Dolby MS12-D **Optional**,
Dolby MS12-Y **Optional**, Dolby MS12-Z **Optional**, and
DTS M6 **Optional**, DTS M6 multistream
decoder/encoder
- Supports Audio Description
- Supports MPEG audio encoding
- Supports time-shifting PVR
- Supports programmable delay for
audio/video synchronization

Audio Interface

- One L/R audio line-input
- One L/R output for main speaker or
additional
line-output
- Supports stereo headphone driver
- I2S digital audio output
- S/PDIF digital audio output and
input **optional**
- Supports HDMI receiver ARC function
- Supports PDM input for 2/4 channels
digital
- Microphone

Analog RGB Compliant Input Ports

- One analog ports support up to 1080P
- Supports PC RGB input up to
SXGA@75Hz
- Supports HDTV RGB/YPbPr/YCbCr
- Supports Composite Sync and SOG Sync-
on-
- Green
- Automatic color calibration

Analog RGB Auto-Configuration & Detection

- Auto input signal format and mode
detection
 - Auto-tuning function including phasing,
- Automatic 3:2/2:2/M:N Pull-Down
- Detection and Recovery
MediaTek Genuine 3D
- Supports Mandatory 3D Format
Backlight Technology
- Supports Direct and Edge Types Local
Dimming
- Programmable Light Spread Profile
- Content Adaptive LCD Backlight Control

- positioning, offset and gain configuration
- Sync Detection for H/V Sync

DVI/HDCP/HDMI Compliant Input Ports

- Three HDMI/DVI input ports
- HDMI 1.4b Compliant
- MediaTek iSwitch for fast HDMI switching
- HDCP 2.2/1.4 Compliant
- Supports HDMI CEC
- Supports HDMI ARC TX
- Robust receiver with excellent long-cable
Support

MediaTek High Performance Video Processor

- Video Processing Engine
 - Supports up to 2K FHD@60p
 - 10/12-bit Internal Data Processing
 - Arbitrary Frame Rate Conversion
 - Video Care Technology
 - Video Line Broken Artifact Detection and
Removal
 - Video Detection & Repairing Technology
for Lousy Inputs such as Internet Streaming
Fully Programmable Multi-Function Scaling
 - Engine
 - High-Quality Filters with Programmable
Parameter
 - An advanced Zoom Algorithm providing
Aliasing/Ringing Suppression
 - Nonlinear Video Scaling supports various
modes including Panorama
 - Supports Dynamic Scaling for RM, VC-1
 - Fully Programmable Zoom Ratios for
Up/Down Scaling
 - Independent Horizontal and Vertical Zoom
Deinterlacer
 - Motion Compensated Video Deinterlacing
with Motion Object Stabilizer
 - Motion Adaptive Deinterlacer
 - Edge-Oriented Deinterlacer with Edge
Smoothing and Artifact Removal
- High Dynamic Range
 - Supports SMPTE ST-2084/ST-2086
 - Supports ARIB STD-B67(Hybrid Log
Gamma)/BT.2100
 - Supports 2094-40 (HDR10 plus)
 - Supports ITU-R BT.2100
 - Full HD Premium Ready
 - Dolby Vision
Response Time Compensation
 - Supports Overdrive Technology

MediaTek Professional PQ Engine

UltraClear

– MPEG Artifact Removal

- ☐ Advanced Adaptive Block Noise Reduction

- ☐ Advanced Mosquito Noise

Cancellation

– UltraClear Noise Reduction

- ☐ 3D Motion-Estimation Temporal Filtering

– 3D Noise Reduction

- ☐ 3D Temporal Noise Reduction for Lousy Air/Cable Input

S-Powers

– Video Enhancement Processor

- ☐ Advanced 3D Independent Multi-Band Control Sharpness

Technology

- ☐ Advanced Video Enhancement

Algorithm provides

Aliasing/Ringing Suppression

- ☐ Advanced Chroma Transient

Improvement

- ☐ Supports Luma Transient

Improvement

– Super Resolution

- ☐ Local Detail Enhancement

- ☐ SuperiorClear Multi-Directional

Anti-Aliasing and Jagged

Compensation Technology

- ☐ SuperiorClear Enhance

Management

MACE

– MediaTek Advanced Color Engine

- ☐ MediaTek Graffito Color Manager

- ☐ Color Stain Removal Technology

– Standard Color Format and Processing

- Fully Programmable Input/Output
- CSC
- BT601, BT709, BT2020 (CL/NCL)
- xvYCC601, xvYCC709
- AdobeRGB, AdobeYCC601
- sRGB, sYCC601
- Fully Programmable 12-bit RGB
- Gamma

– Gamut Mapping

- ☐ Nonlinear/Linear RGB Domain

Gamut Mapping

- ☐ Supports 2D Gamut Mapping

- ☐ Supports 3D Gamut Mapping

Luce

– Contrast Enhancement

- ☐ Real-Time Content Adaptive

Contrast Enhancement with Chroma Compensated

- ☐ Ultra Contrast Dimming

– SDR to HDR

Output Interface

- Single/Dual link 8/10-bit LVDS output
- Supports panel resolution up to Full HD
- 1920x1080@60Hz (LVDS 2ch)
- Supports TCON:miniLVDS 2ch interface, panel resolution up to Full HD@60Hz**optional**
- Supports TCON:EPI interface, panel resolution up to Full HD@60Hz**optional**
- Supports TTL output, update to
- 1920x1080@60Hz
- Supports programmable timing controller
- Supports dithering options
- Spread spectrum output frequency for EMI suppression
- Supports 60Hz 3D polarized panel (line interleave)
- Supports Cinema output mode

CVBS Video Encoder

- Supports all NTSC/PAL TV Standard
- Stand-alone scaling engine (no vertical scaling up)
- Programmable Hue, Contrast, Brightness
- Supports TTX/WSS output

CVBS Video Output

Allows CVBS output of digital content to SCART

2D Graphics Engine

- Hardware Graphics Engine for responsive interactive applications
- Supports line draw, rectangle draw/fill and text draw
- Supports BitBlt, Stretch BitBlt, Italic Bitblt, Mirror BitBlt and Rotate BitBlt
- Supports alpha-blending operation
- Supports source/destination color key and alpha key
- Supports dither
- Supports color format conversion and format

- transformation
- Raster Operation (ROP)
- Supports DFB and Porter-Duff operation

VIF Demodulator

- Compliant with NTSC M/N, PAL B, G/H, I, D/K,
- SECAM L/L' standards
- Supports low IF architecture
- Audio/Video internal dual-path processor
- Locking range improvement

ATSC/QAM Demodulator

- ATSC A/53 compliant 8VSB
- ITU-T J.83 Annex B, SCTE DVS-031 compliant
- 64/256QAM receiver
- 2010 - A74 compliant
- All digital demodulation and timing recovery
- loops for tracking frequency and clock offset
- Automatic co-channel and adjacent channel interference suppression
- Impulse-Noise suppression
- Integrated deinterleaver RAM for Level 1 J=1 and Level 2 J= 1,2,3,4
- Supports LIF interfaces

ISDB-T DemodulatorOptional

- Compliant with ISDB-T ARIB STD-B31
- Compliant with ISDB-Tsb ARIB STD-B29
- Supports all modes defined in ISDB-T specs
- Supports all guard ratios: 1/4, 1/8, 1/16, 1/32
- Support LIF interfaces
- Impulse-noise suppression
- Phase noise compensation
- Outside-GI performance improvement
- CNR performance improvement

DVB-C Demodulator

- Compliant with ITU J.83 Annex A/C DVB-C (EN 300 429)
- Supports 1-7.2 M Baud symbol rate
- Automatic blind channel scan (constellation and symbol rate)
- Supports LIF interfaces

- IIS performance improvement

DVB-T Demodulator

- Compliant with DVB-T (ETSI EN 300 744)
- Nordig 2.2.2, D-book 7.0 compliant
- Accept low IF inputs in 6, 7, 8MHz channel bandwidths
- Supports all guard intervals (1/32 to 1/4)
- Supports all constellations (QPSK, 16-QAM, 64-QAM)
- Ultra fast automatic blind UHF/VHF channel scan
- Optimized for SFN channels with pre/postcursive
- echoes inside/outside the guard
- Phase-Noise suppression
- Impulse-Noise suppression
- All digital demodulation and timing recovery
- loops for tracking frequency and clock offset
- Automatic co-channel and adjacent channel interference suppression
- CNR performance improvement
- Outside-GI performance improvement
- DVB-T2 Demodulator **Optional**
- Compliant with DVB-T2 (ETSI EN 302 755)
- v1.3.1, T2-base & T2-Lite profile
- Nordig Unified 2.2.2, D-Book 7.0 compliant
- Supports all guard intervals (1/128 to 1/4)
- Supports all FFT modes from 1K to 32K
- Supports all long and short block code rates (1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 2/5, 1/3)
- Supports all constellations (QPSK, 16-QAM, 64-QAM, 256-QAM)
- Transmit diversity (MISO) support
- Supports all scattered pilot patterns (PP1 to PP8)
- Supports rotated and non-rotated constellations
- Supports single and multiple PLPs
- Accept low IF inputs in 1.7, 5, 6, 7, 8MHz channel bandwidths

- All digital demodulation and timing recovery
- loops for tracking frequency and clock offset
- Automatic co-channel and adjacent channel interference suppression
- Impulse-Noise suppression
- Outside GI improvement
- Locking time improvement

DVB-S DemodulatorOptional

- Compliant with DVB-S (ETSI EN 300 421)
- Data Rate: 1-70 Msps
- Code Rates: 1/2, 2/3, 3/4, 5/6, 7/8
- Carrier frequency acquisition range: 5MHz
- Fast automatic blind scan of symbol rates and carrier frequencies
- Equalizer compensates for channel impairment
- DiSeqCTM 2.0 compatible with LNB controller
- Automatic co-channel and adjacent channel interference suppression
- Impulse-Noise suppression
- All digital demodulation and timing recovery
- loops for tracking frequency and clock offset
- Novel carrier recovery algorithms for tracking and compensating large phase noises
- Supports Automatic FEC and Modulation
- Integrated FEC decoders for near Shannon limit performances
- Integrated signal quality and BER monitors
- Improved CNR performance

DVB-S2 DemodulatorOptional

- Compliant with DVB-S2 (ETSI EN 302 307)
- Data Rate: 1-70 Msps for QPSK , 8PSK, 16APSK, 1-57 Msps for 32APSK
- Constellations: QPSK , 8PSK , 16APSK and 32APSK
 - QPSK Code Rates: 1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 8/9, 9/10
 - 8PSK Code Rates: 3/5, 2/3, 3/4, 5/6, 8/9,

9/10

- 16APSK Code Rates: 2/3, 3/4, 4/5, 5/6, 8/9,

9/10

- 32APSK Code Rates: 3/4, 4/5, 5/6, 8/9, 9/10

- Supports CCM and VCM
- Supports Single Transport Stream and Multiple Transport Streams
- Roll-off factors for pulse shaping: 0.2, 0.25, and 0.35
- Carrier frequency acquisition range: 5MHz
- Fast automatic blind scan of symbol rates and carrier frequencies
- Equalizer compensates for channel impairment
- DiSeqCTM 2.0 compatible with LNB controller
- Automatic co-channel and adjacent channel interference suppression
- Impulse-Noise suppression
- All digital demodulation and timing recovery
- loops for tracking frequency and clock offset
- Novel carrier recovery algorithms for tracking and compensating large phase noises
- Supports Automatic FEC and Modulation
- Integrated FEC decoders for near Shannon limit performances
- Integrated signal quality and BER monitors

DVB-S2X DemodulatorOptional

- Compliant with DVB-S2 Extensions (ETSI EN 302 307-2, Broadcast services except for Channel Bonding)
- Data Rate: 1-70 Msps for QPSK , 8PSK, 8APSKL, 16APSK, 16APSK-L, 1-57 Msps for 32APSK, and 32APSK-L
- Constellations: QPSK , 8PSK, 8APSK-L, 16APSK, 16APSK-L, 32APSK, and 32APSK-L
 - QPSK Code Rates: 1/4, 1/3, 2/5, 1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 8/9, 9/10, 13/45, 9/20, 11/20
 - 8PSK Code Rates: 3/5, 2/3, 3/4, 5/6, 8/9, 9/10, 23/36, 25/36, 13/18

- 8APSK-L Code Rates: 5/9, 26/45
- 16APSK Code Rates: 2/3, 3/4, 4/5, 5/6, 8/9, 9/10, 26/45, 3/5, 28/45, 23/36, 25/36, 13/18, 7/9, 77/90
- 16APSK-L Code Rates: 5/9, 8/15, 1/2, 3/5, 2/3
- 32APSK Code Rates: 3/4, 4/5, 5/6, 8/9, 9/10, 32/45, 11/15, 7/9
- 32APSK-L Code Rates: 2/3
- Supports CCM and VCM
- Supports Single Transport Stream and Multiple
- Transport Streams
- Roll-off factors for pulse shaping: 0.05, 0.1, 0.15, 0.2, 0.25, and 0.35
- Carrier frequency acquisition range: 5MHz
- Fast automatic blind scan of symbol rates and
- carrier frequencies
- Equalizer compensates for channel
- impairment
- DiSEqCTM 2.0 compatible with LNB controller
- Automatic co-channel and adjacent channel
- interference suppression
- Impulse-Noise suppression
- All digital demodulation and timing recovery

- loops for tracking frequency and clock offset
- Novel carrier recovery algorithms for tracking
- and compensating large phase noises
- Supports Automatic FEC and Modulation
- Integrated FEC decoders for near Shannon
- limit performances
- Integrated signal quality and BER monitors

Connectivity

- Three USB 2.0 host ports
- USB architecture designed for efficient support of external storage devices in conjunction with off air broadcasting
- Embedded 10/100 Ethernet PHY
- Supports Ethernet Wake-On-Lan

Miscellaneous

- DRAM interface support DDR3
- Supports PVR
- Parallel interface for external parallel eMMC
- flash and NAND flash support
- Power control module with ultra low power
- MCU available in standby mode
- 462-ball BGA package
- Operating Voltages: TBD

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
3.3V Supply Voltages	V _{VDD_33}	3.14	3.3	3.46	V
1.5V Supply Voltages (DDR3)	V _{VDD_15}	1.43	1.5	1.57	V
Core Supply Voltages	V _{VDD_core}	TBD			V
		TBD			V
CPU Supply Voltages	V _{VDD_cpu}	TBD			V
		TBD			V
Ambient Operating Temperature	T _A	0		70	°C
Junction Temperature	T _J			125	°C

Table 6: Recommended Operating Conditions

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
3.3V Supply Voltages	V_{VDD_33}		3.63	V
1.5V Supply Voltages	V_{VDD_15}		1.65	V
Core Supply Voltages	V_{VDD_core}		TBD	V
CPU Supply Voltages	V_{VDD_cpu}		TBD	V
Input Voltage (5V tolerant inputs)	$V_{IN5Vtol}$		5.3	V
Input Voltage (non 5V tolerant inputs)	V_{IN}		V_{VDD_33}	V
Storage Temperature	T_{STG}	-40	150	°C
Junction Temperature	T_J		150	°C

Table 7: Absolute Maximum Ratings

7.4 GB EMMC

SKYHIGH EMMC 4GB S40FC004 (U108)

Description

SkyHigh e.MMC is a managed NAND memory solution designed for embedded applications. SkyHigh e.MMC includes a flash controller and a standard MLC NAND flash memory, and is compatible with the JEDEC JESD84-B451 with backwards compatibility to previous e.MMC specifications. Designed for faster throughput and large data transfer, SkyHigh e.MMC offers high performance, great reliability, and minimal latency.

In addition to higher performance, SkyHigh's e.MMC offers optimum power management features resulting in reduced power consumption, making it an ideal solution for mobile applications.

In addition, highly optimized SkyHigh firmware fully utilizes the MLC NAND capabilities leveraging wear-leveling, defect management, garbage collection, and ECC to enhance product life. The SkyHigh e.MMC product family offers a vast array of the JEDEC e.MMC features including HS200, HS400, high priority Interrupt (HPI), boot partitions, RPMB partitions, background operations, hardware reset, and power off notification. Combined with an advanced e.MMC feature set and SkyHigh's commitment to quality, SkyHigh e.MMC is ideal for industrial applications as well as set top boxes, gaming consoles, and consumer electronic devices.

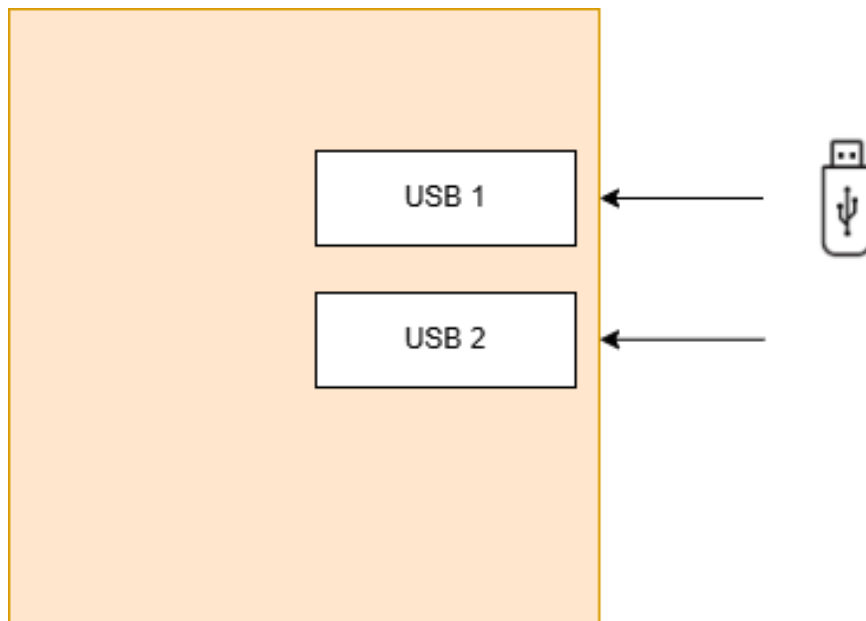
Features

- **e.MMC 5.1 Specification Compatible**
 - Backward compatible with previous e.MMC specifications
- **Storage Temperature**
 - -40°C to $+85^{\circ}\text{C}$
- **Operating Voltage**
 - V_{CCQ} : 1.7V - 1.95V or 2.7V - 3.6V
 - V_{CC} : 2.7V - 3.6V
- **Density: 4 / 8 / 16 GB of Data Storage**
- **Data Bus Width:**
 - SDR Mode: 1 bit, 4 bit, 8 bit
 - DDR Mode: 4 bit, 8 bit
 - HS200 Mode: 4 bit, 8 bit
 - HS400 Mode: 8 bit

- **Clock Frequency: 52 MHz, 200 MHz**
 - SDR Mode: up to 52 MHz
 - DDR Mode: up to 52 MHz
 - HS200 Mode: up to 200 MHz
 - HS400 Mode: up to 200 MHz
- **BGA Packages**
 - 153-ball VFBGA — 13 mm x 11.5 mm x 1.0 mm

- **Operating Temperature Range**
 - Commercial (0°C to $+70^{\circ}\text{C}$)
 - Industrial (-40°C to $+85^{\circ}\text{C}$)

8. USB INTERFACE



USB POWER SWITCH JW7111SOTE (U107)

DESCRIPTION

The JW[®]7115/JW7115-1/JW7115-2/JW7111 is a single channel current-limited power switch optimized for Universal Serial Bus (USB) and other hot-swap applications. The rise and fall times are controlled to minimize current overshoot or undershoot during switches on/off.

The device has fast short-circuit response time for improved overall system robustness. It provides a complete protection solution, such as over-current protection, over-temperature protection and short-circuit protection, as well as controlled rise time and under-voltage lockout function. A 7.5ms de-glitch time on the open-drain Flag output prevents false over-current reporting.

JW7115/JW7115-1/JW7115-2 offers SOT23-5 package. JW7111 offers both DFN2X2-6 and SOT23-6 packages.

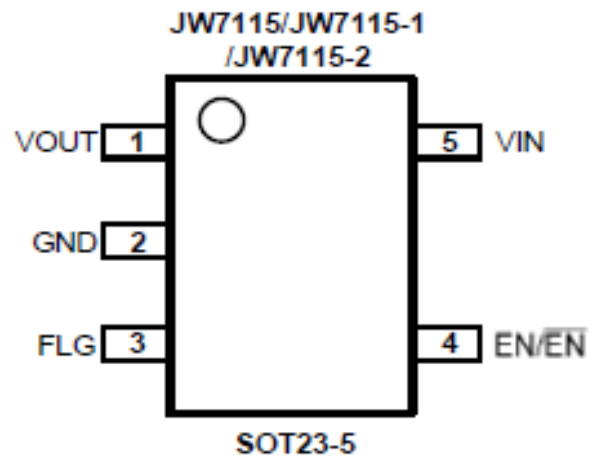
Company's Logo is Protected, "JW" and "JOULWATT" are Registered Trademarks of JoulWatt technology Inc.

FEATURES

- 50mΩ Integrated N-MOSFET Switch
- Accurate Current Limit
- FLG: active low
- Constant-Current During Over-Current
- Fast Short-Circuit Response Time: 2μs (typ.)
- Operating Range: 2.7V - 5.5V
- Built-in Soft-Start with 3ms Typical Rise Time
- Over-Current, Output Over-Voltage and Thermal Protection
- Fault Report (FAULT) with De-glitch Time
- UL Recognized, File Number E497605
- IEC Recognized, File Number DK-69902-UL
- ESD Protection: 2kV HBM, 500V CDM
- Available in SOT23-5, SOT23-6 and DFN2X2-6 Packages

APPLICATIONS

- Set-Top Boxes
- LCD TVs & Monitors
- Residential Gateways
- Laptops, Desktops, Servers, e-books, Printers, Docking
- Stations, HUBs



9. CI INTERFACE

TPS 563203 Digital CI Interface Block diagram:

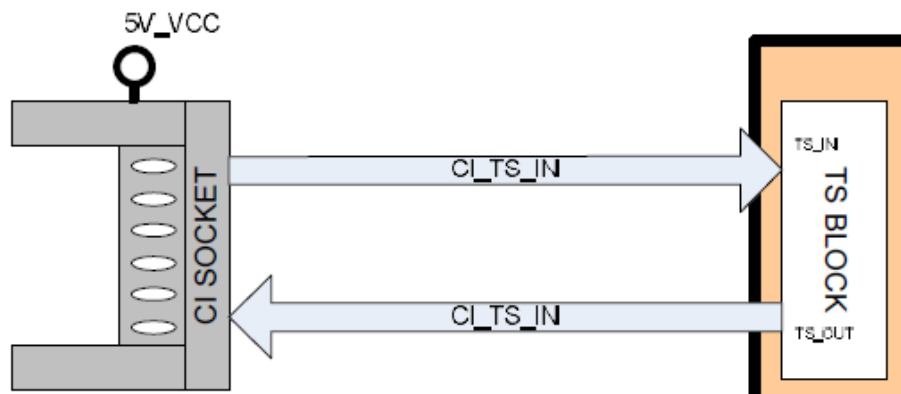


Figure 11: CI interface

10. WI-FI IC

1.1 General Descriptions

The MT7601U is a highly integrated Wi-Fi single chip which supports 150 Mbps PHY rate. It fully complies with IEEE 802.11n and IEEE 802.11 b/g standards, offering feature-rich wireless connectivity at high standards, and delivering reliable, cost-effective throughput from an extended distance.

Optimized RF architecture and baseband algorithms provide superb performance and low power consumption. Intelligent MAC design deploys a high efficient DMA engine and hardware data processing accelerators which offloads the host processor.

The MT7601U is designed to support standard based features in the areas of security, quality of service and international regulations, giving end users the greatest performance any time and in any circumstance.

1.2 Features

1.2.1 Platform

- Embedded high-performance 32-bit RISC microprocessor
- Highly integrated RF with 55nm CMOS technology
- Integrate high efficiency switching regulator
- Best-in-class active and idle power consumption performance
- Compact 5mm x 5mm QFN40L package
- 1/2/3/4-wire PTA WiFi / Bluetooth coexistence
- Buffered clock output for co-clock with other SOC chipset
- Integrate EFUSE to eliminate the requirement for external EEPROM
- External serial flash support
- 7 programmable general purpose Input / Output
- 2 configurable LED pins
- Fully compliance with USB v2.0 High-speed mode
- Auto-calibration

1.2.2 WLAN

- IEEE 802.11 b/g/n compliant
- 1T1R mode with support of 150Mbps PHY rate
- Greenfield, mixed mode, legacy modes support
- Frame aggregation
- Integrated LNA, PA, and T/R switch
- IEEE 802.11 d/h/k support
- Security support for WPA/WPA2 personal, WPS2.0, WAPI
- Supports 802.11w protected managed frames
- QoS support of WPA WMM, WMM PS
- Supports Wi-Fi Direct

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	PERFORMANCE			
		MIN	TYP	MAX	Unit
Switching regulator					
Input voltage		2.97	3.3	3.63	V
Output voltage	Default voltage setting in the programmable range ¹	1.4	1.5	1.6	V
Output current		-	-	300	mA
Quiescent current		-	-	3.5	mA
Line regulation	3.63V input voltage range @ no load	-	-	1	%
Load regulation	1mA to 300mA load current	-	-	0.05	mV/mA
Efficiency	300mA load current	-	80	-	%
Over-current Shutdown	Threshold	-	600	-	mA
Digital LDO					
Input voltage		1.4	1.5	1.6	V
Output voltage		1.08	1.2	1.32	V
Output current		-	-	200	mA
Quiescent current	No load	-	10	-	uA

Table 11 PMU electrical characteristics

11. SOFTWARE UPDATE

MAIN SOFTWARE UPDATE

In MB181 project, please follow software update procedure:

1. 02_rom_emmc_boot_mb181.bin, mb181_en.bin, usb_auto_update_G36.txt and mboot_emmc_mb181.bin documents should be copied directly inside root of a flash memory (not in a folder).
2. Insert flash memory to the TV when TV is powered off.
3. While pushing the OK button on remote control, then power on and wait. TV will power-up itself.
4. If First Time Installation screen comes, it means software update procedure is successful.

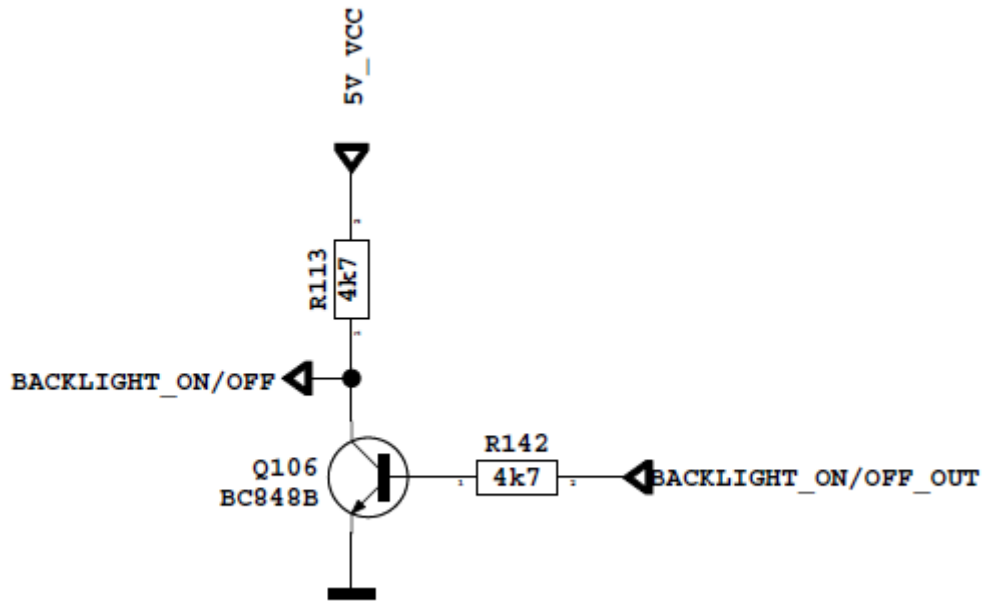
12. TROUBLESHOOTING

A. NO BACKLIGHT PROBLEM

Problem: If TV is working, led is normal and there is no picture and backlight on the panel.

Possible causes: Backlight pin, dimming pin, backlight supply, stby on/off pin

BACKLIGHT_ON/OFF pin should be high when the backlight is ON. Collector pin of Q106 must be low when the backlight is OFF. If it is a problem, please check Q106. Also it can be tested in TP108 in main board. Please also check panel cables.

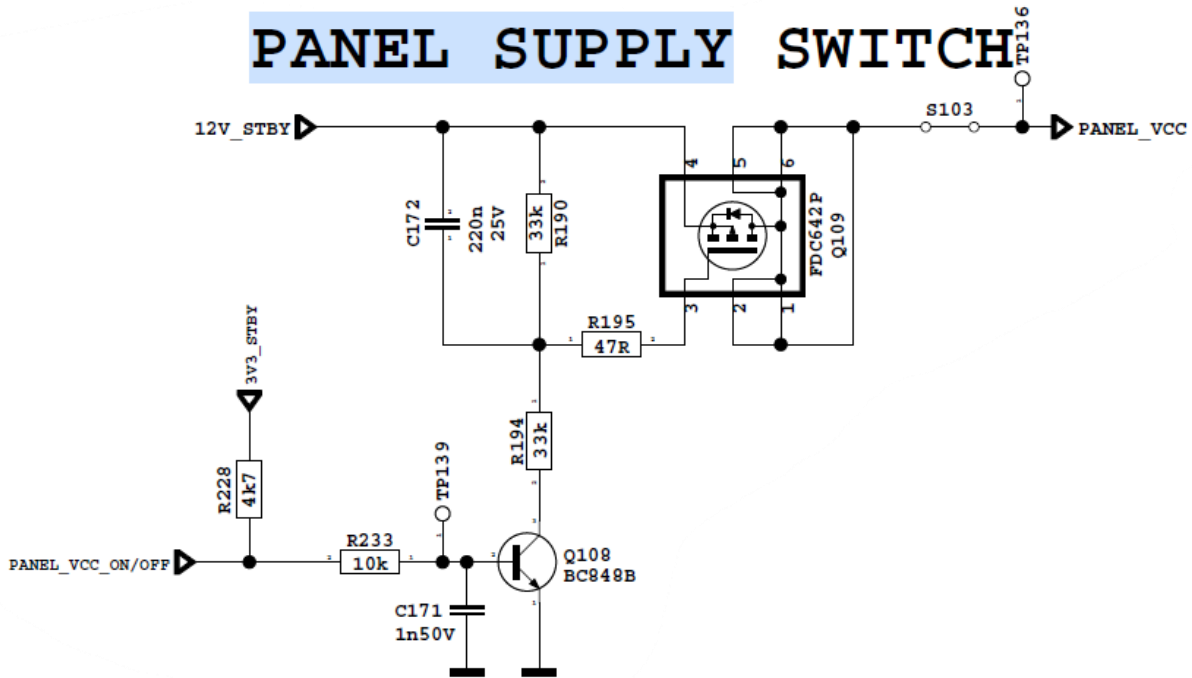


Dimming pin should be high or square wave in open position. It also can be checked at TP119. Please also check panel or power cables and connectors.

Backlight power supply should be in panel specs. Please check Q116, shown below; also it can be checked TP136.

STBY_ON/OFF_NOT should be low for TV on condition, please check Q114's collector.

PANEL SUPPLY SWITCH



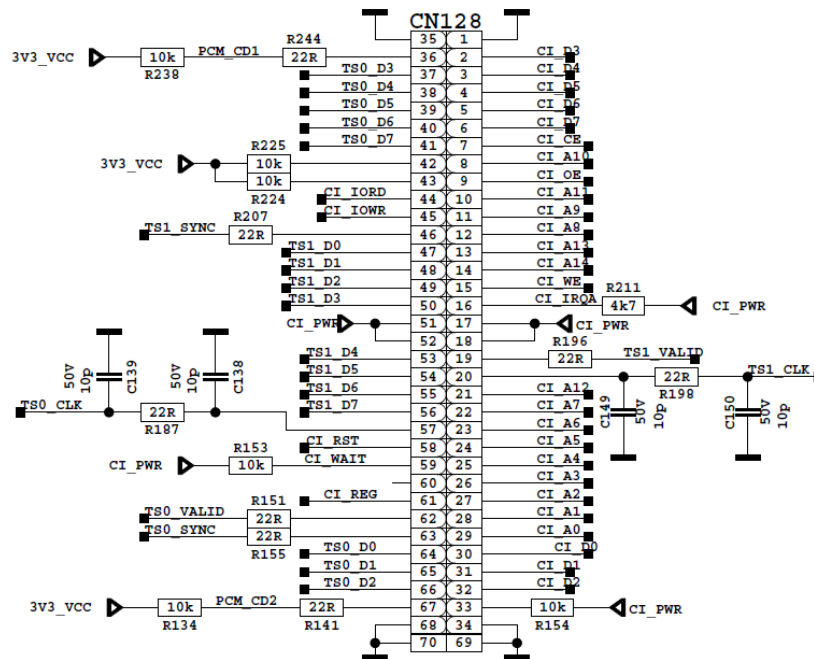
B. CI MODULE PROBLEM

Problem: CI is not working when CI module inserted.

Possible causes: Supply, supply control pin, detects pins, mechanical positions of pins.

- Please check mechanical position of CI module. Is it inserted properly or not?
- Detect ports should be low. If it is not low please check CI connector pins, CI module pins.

CI

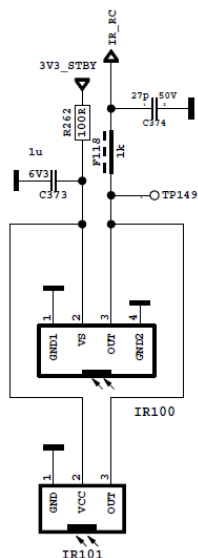


C. IR PROBLEM

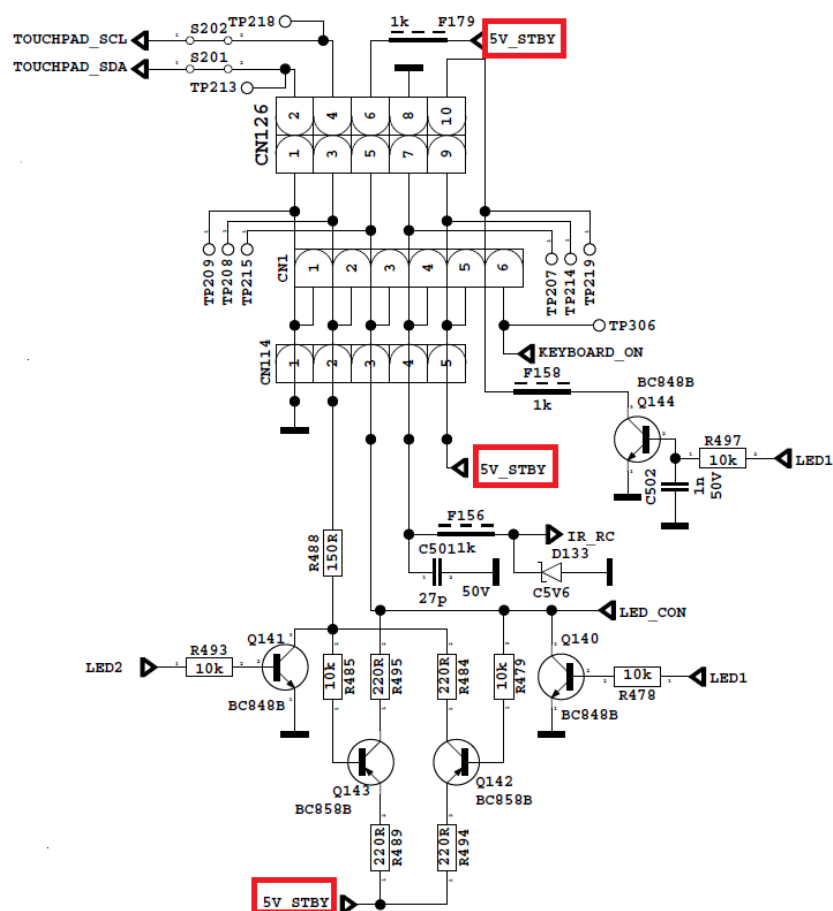
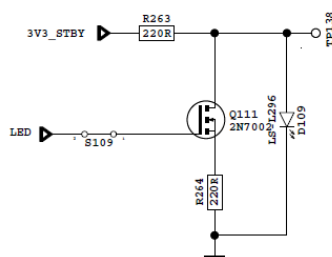
Problem: LED or IR not working

Check LED card supply on MB181 chasis.

IR ONBOARD



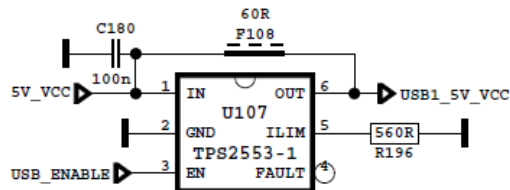
LED ONBOARD



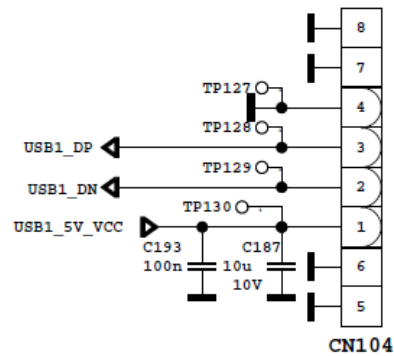
D. USB PROBLEMS

Problem: USB is not working or no USB Detection.

Check USB Supply, It should be nearly 5V. Also USB Enable should be logic high.



USB 2.0



E. NO SOUND PROBLEM

Problem: No audio at main TV speaker outputs.

Check supply voltages of 12V_VCC and AMP_EN with a voltage-meter. There may be a problem in headphone connector or headphone detect circuit. Measure voltage at HP_DETECT pin, it should be 3.3v.

Teraterm program. These printouts may give a clue about the problem. You can use VGA for Teraterm program connection.

G. NO SIGNAL PROBLEM

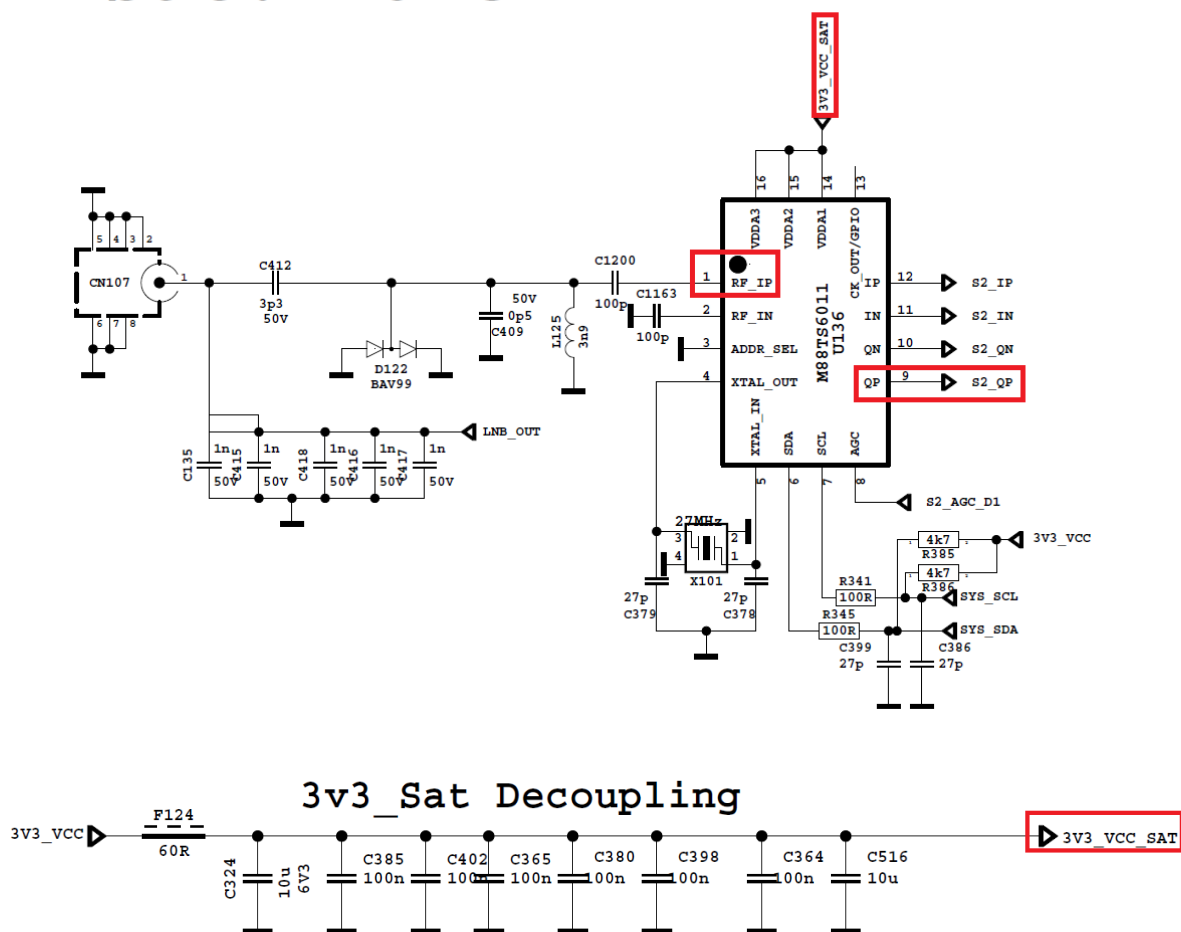
Problem: No signal or Low signal in DVB-S/S2 mode.

Check signal cables and LNB voltage, if there is no problem, check M88TS6011 (U136) supply voltages; 3V3_VCC_SAT.

If the above measurements are OK, then measure the voltage from the PIN1 of U136.

If the PIN9 voltage is equal to 0V, please check i2c waveforms and software. If the PIN9 voltage is lower than 1V(e.g: 0.8V or 0.3V), change the U136 with a new part.

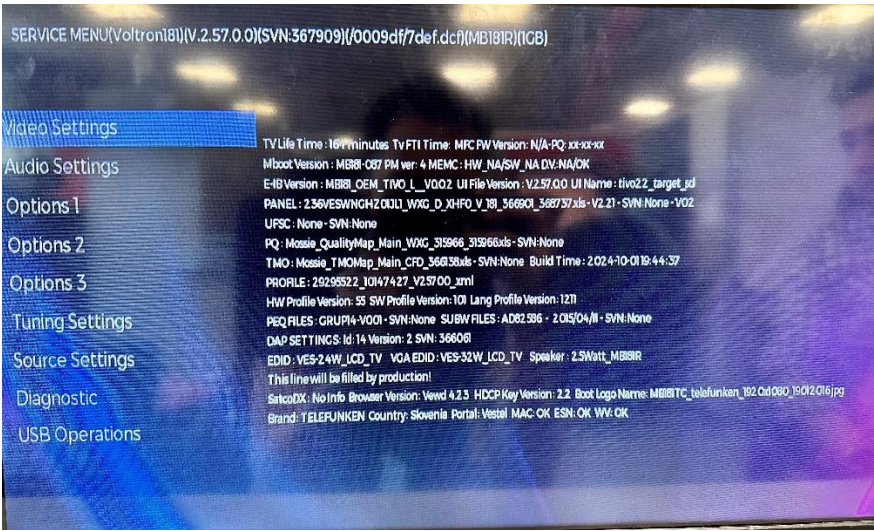
Sat. Tuner



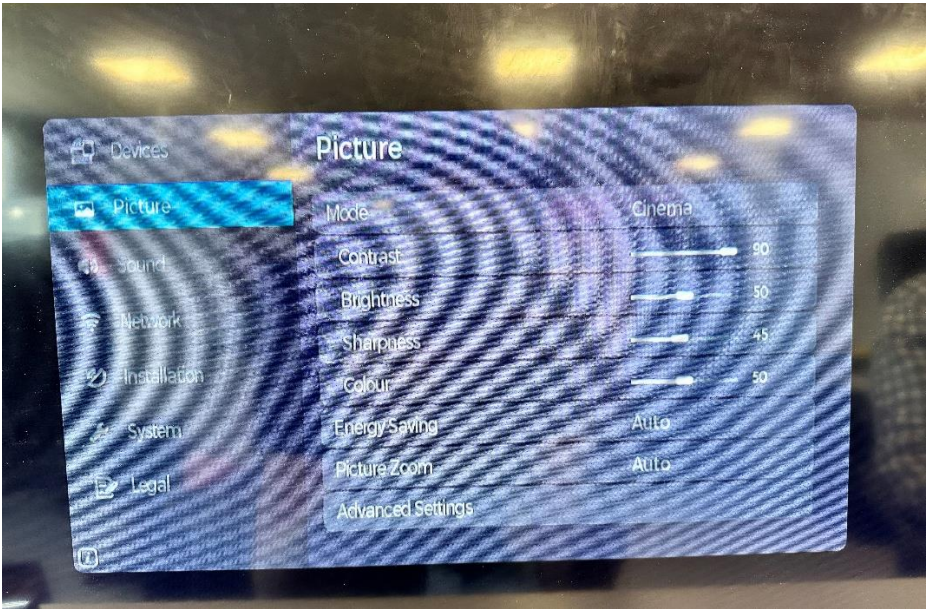
13. SERVICE MENU SETTINGS

In order to reach service menu, first Press “MENU” buton, then write “4725” by using remote controller.

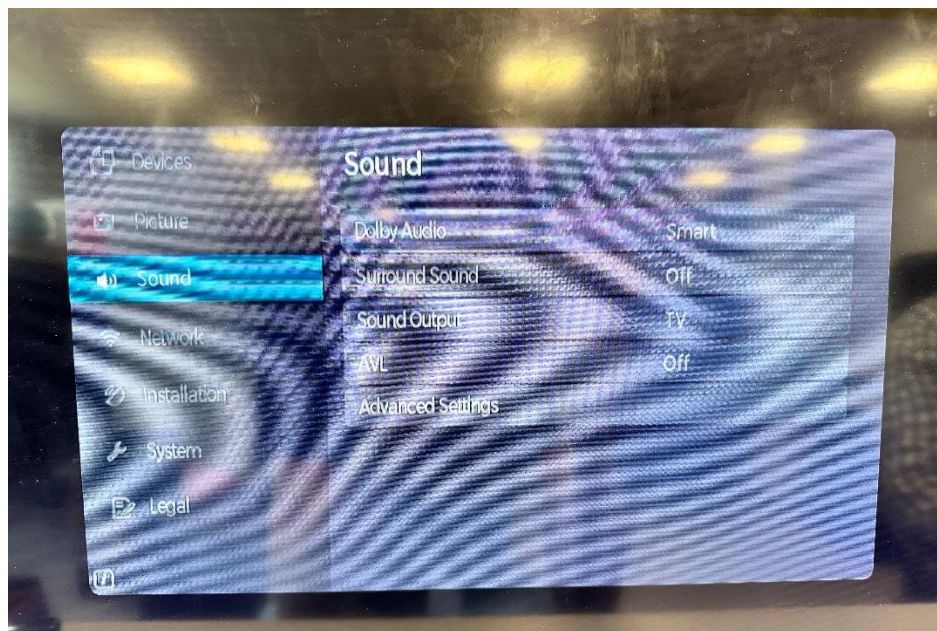
You can see the service menu main screen below. You can check SW releases by using this menu. In addition, you can make changes on video, audio etc. by using video settings, audio settings titles.



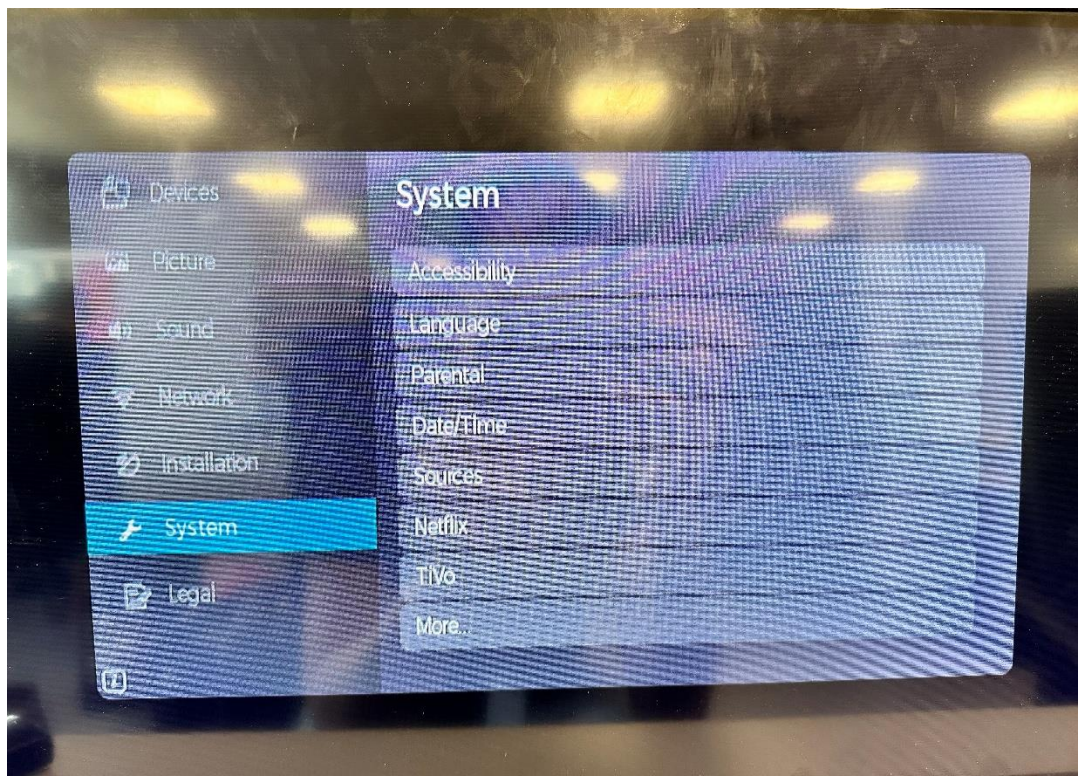
Service Menu



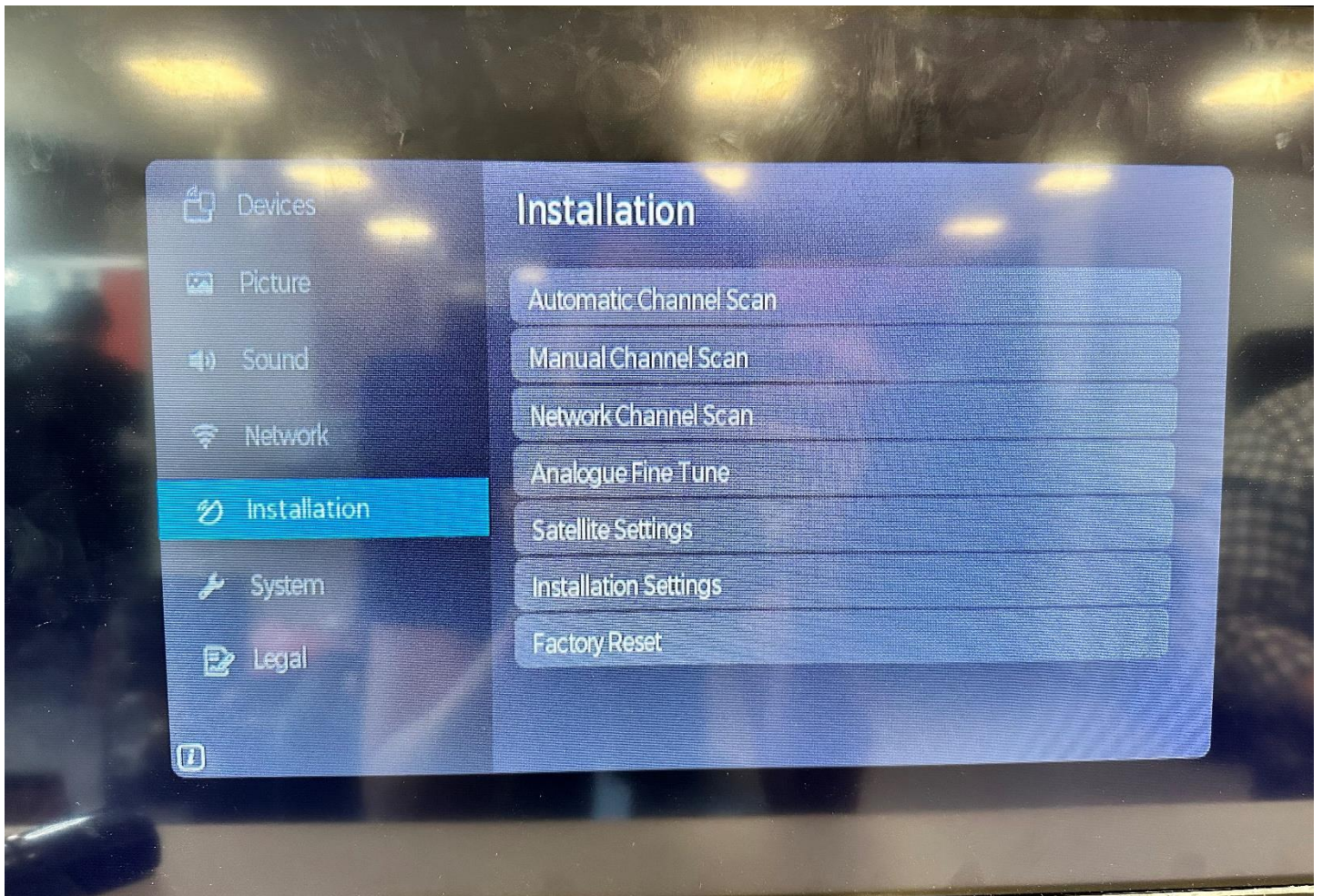
Video Settings



Audio Settings

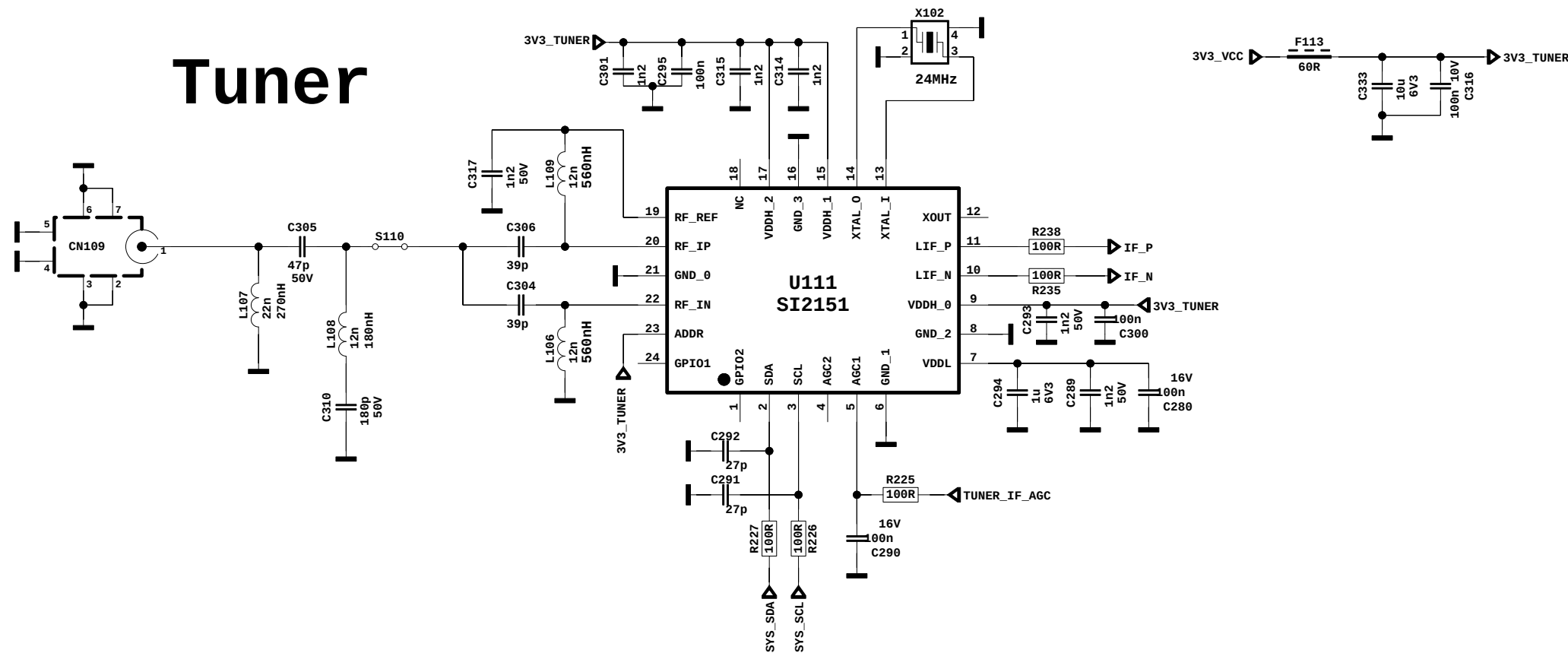


System Settings

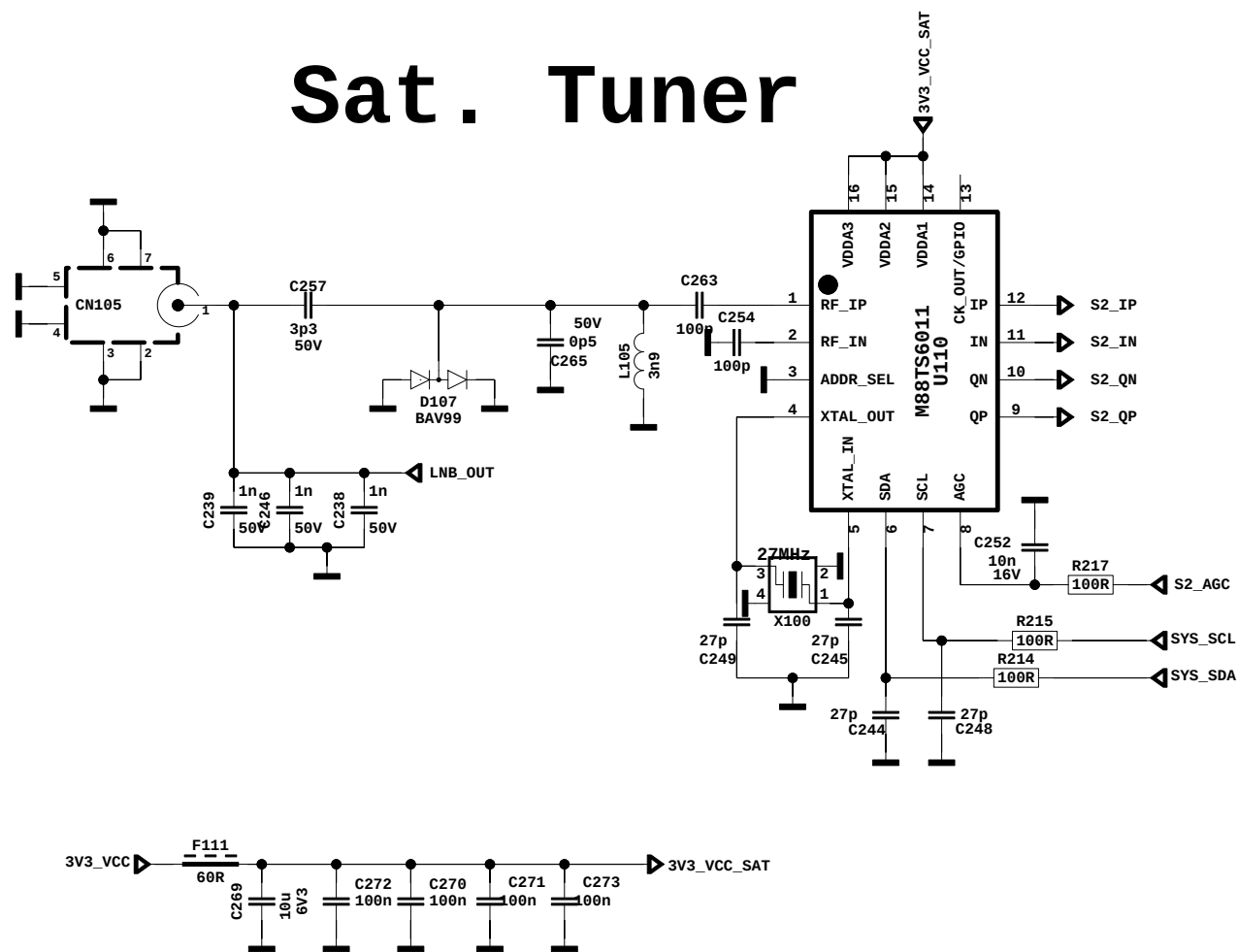


Installation Settings

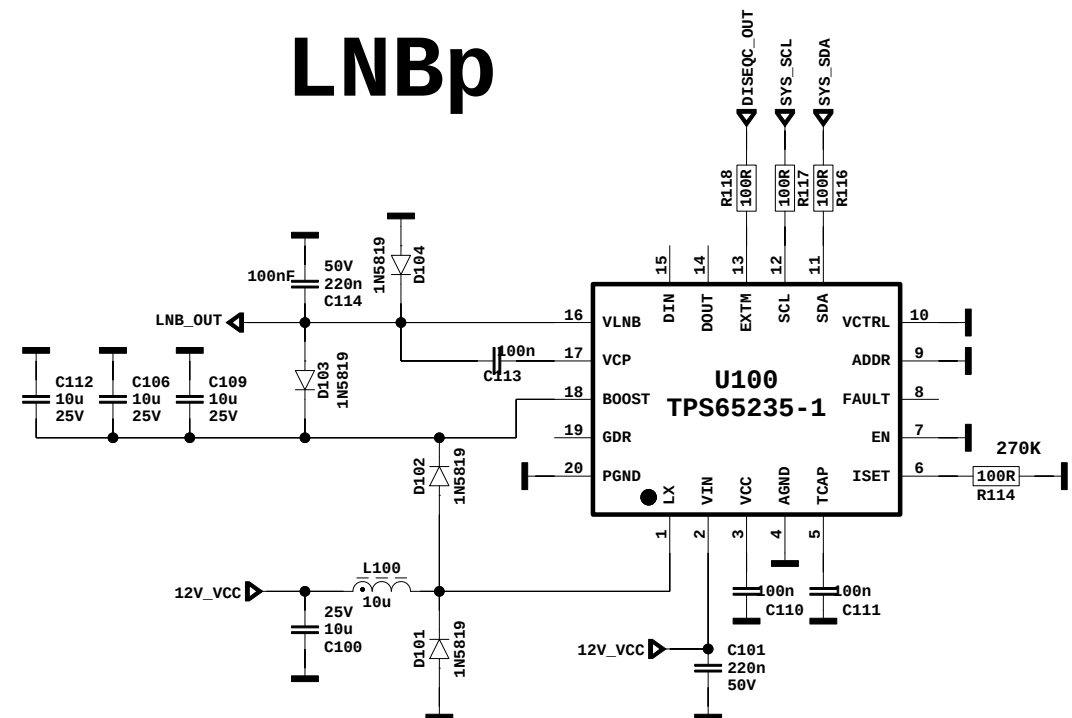
Tuner

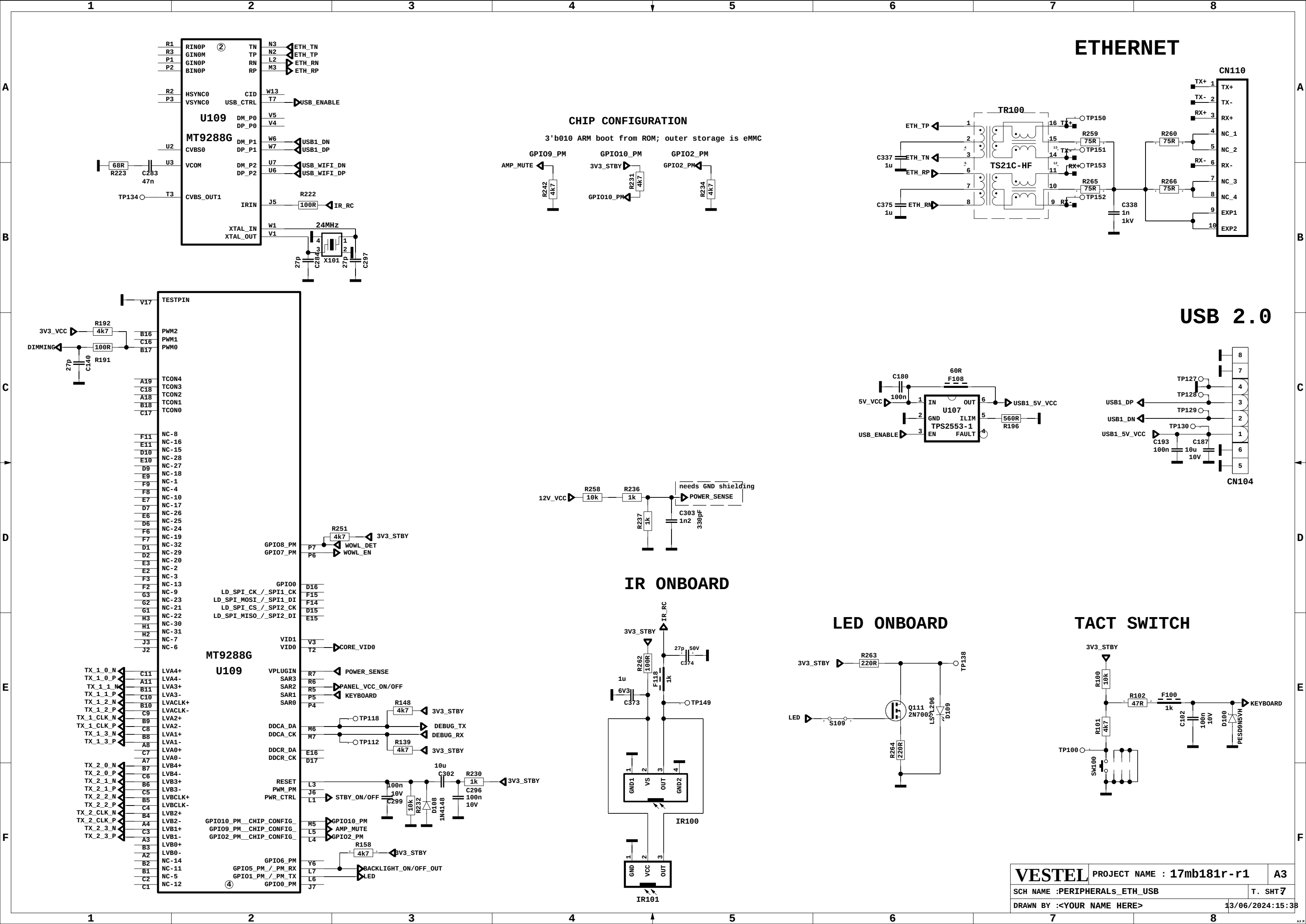


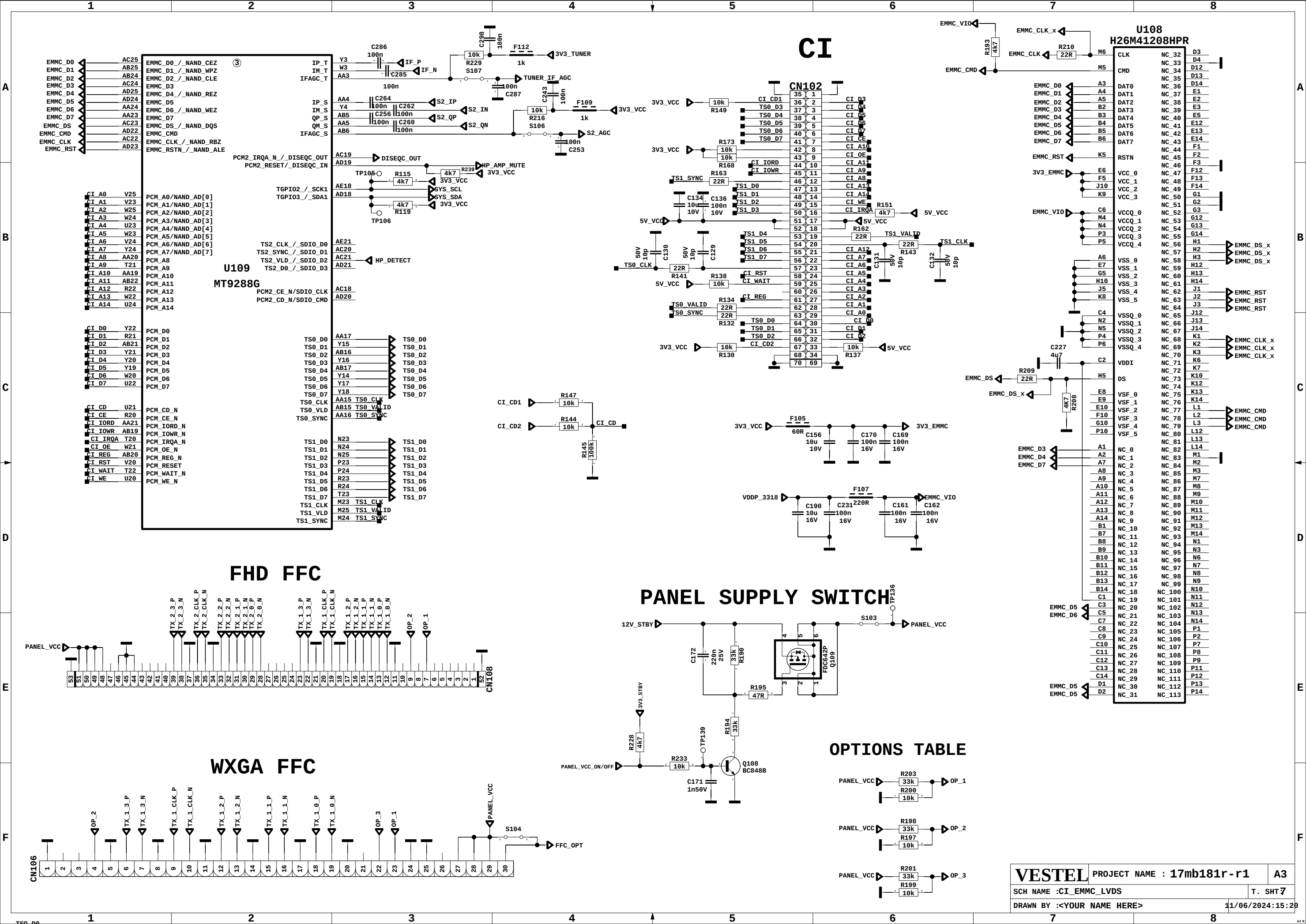
Sat. Tuner



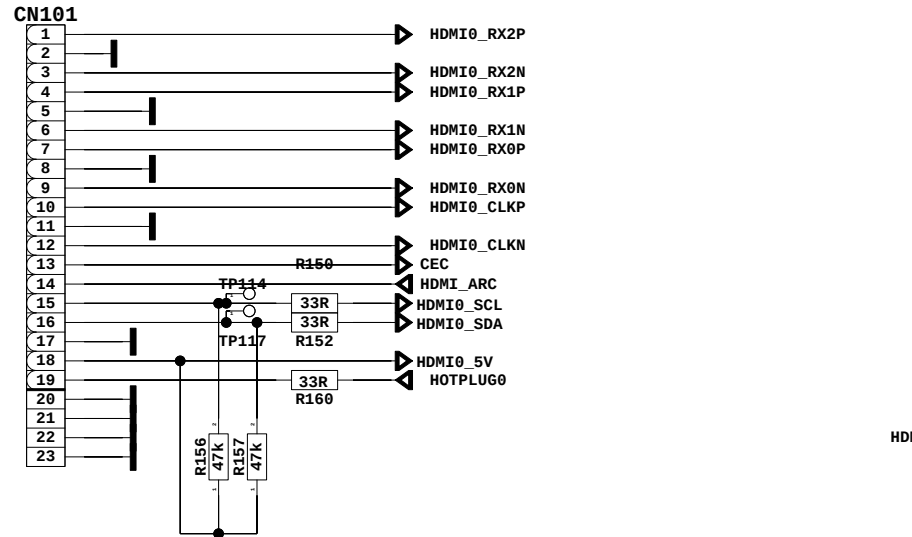
LNBp



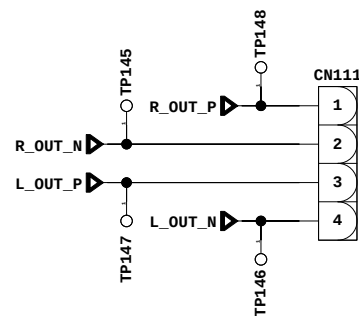
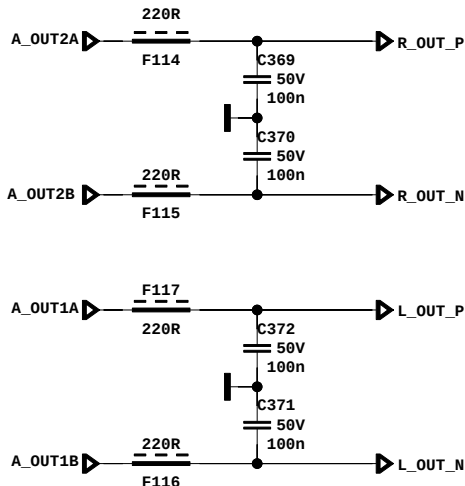
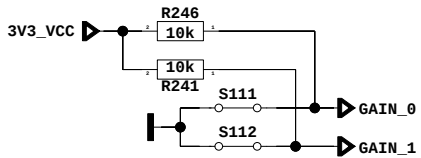
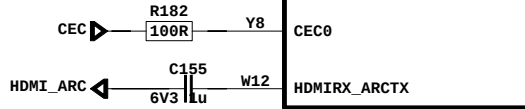
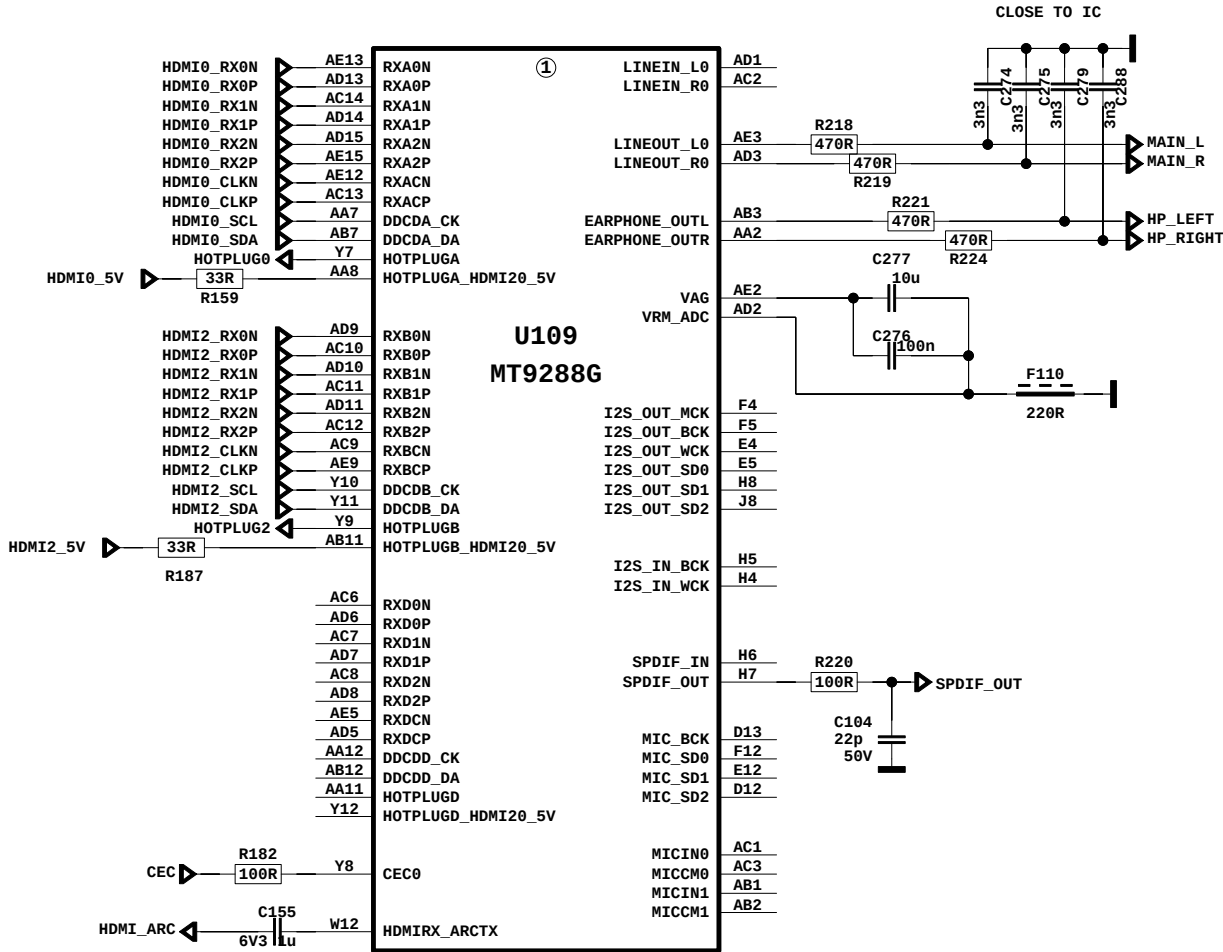
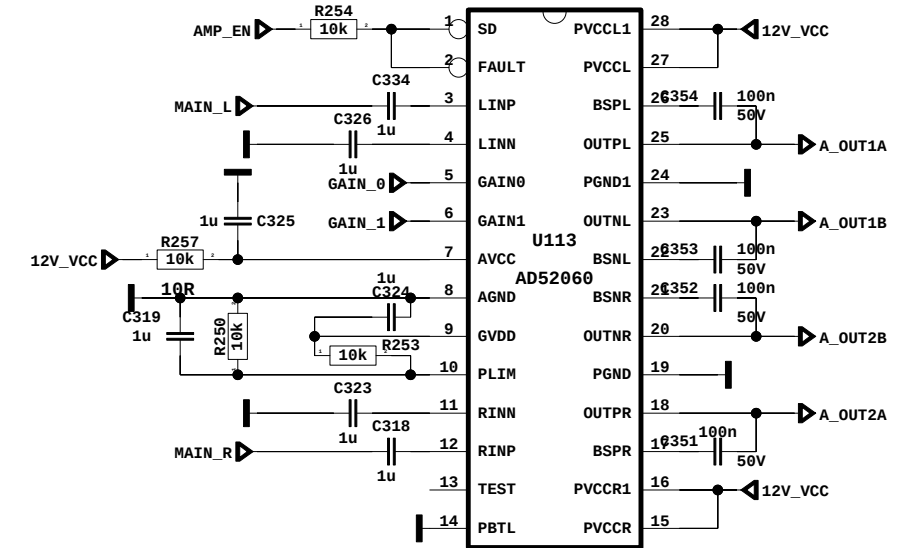
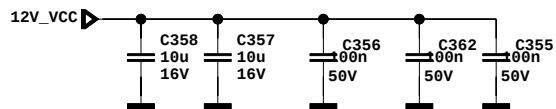
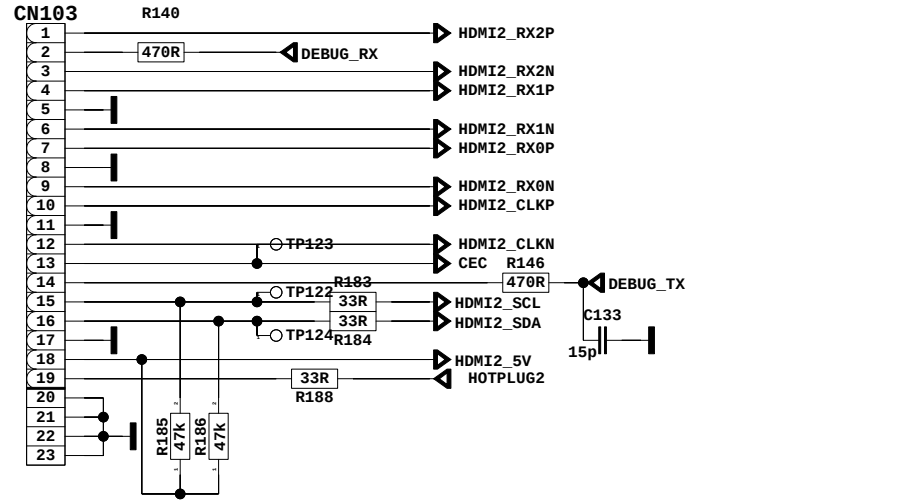




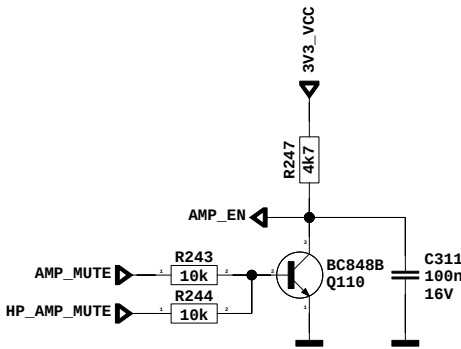
HDMI2 (SIDE-W/ARC)



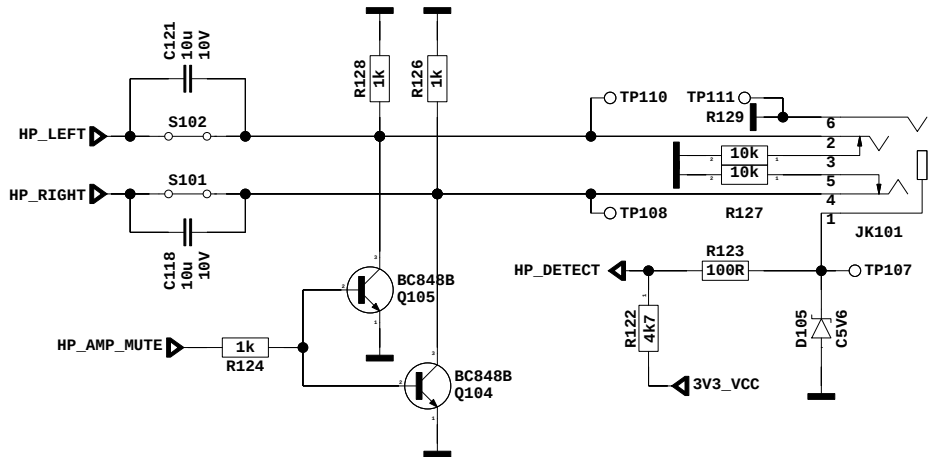
HDMI1 (SIDE)



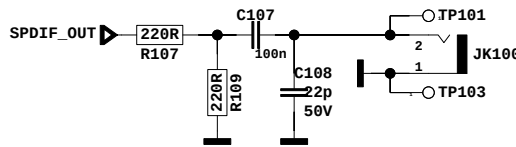
POP NOISE

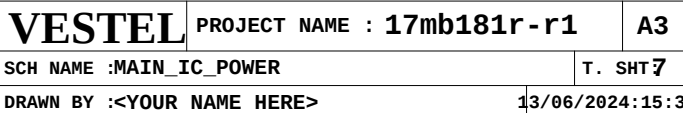


HEADPHONE OUTPUT

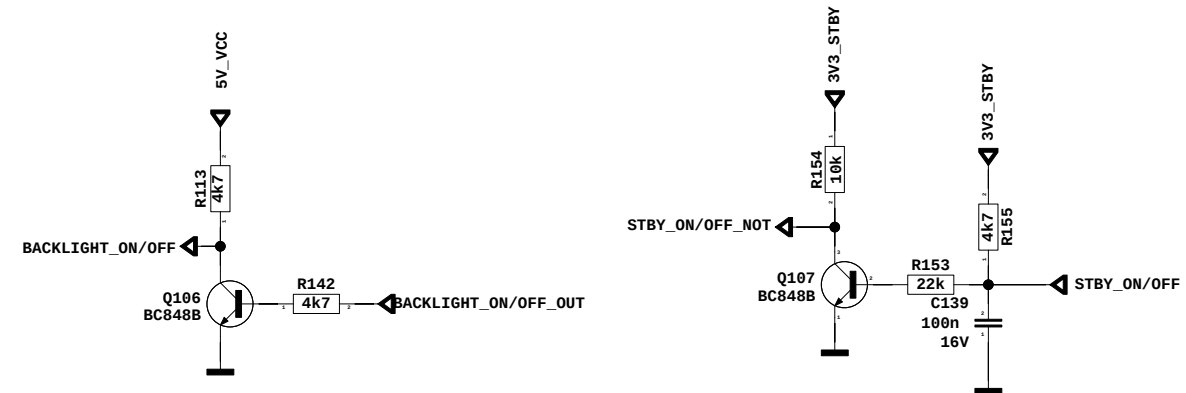
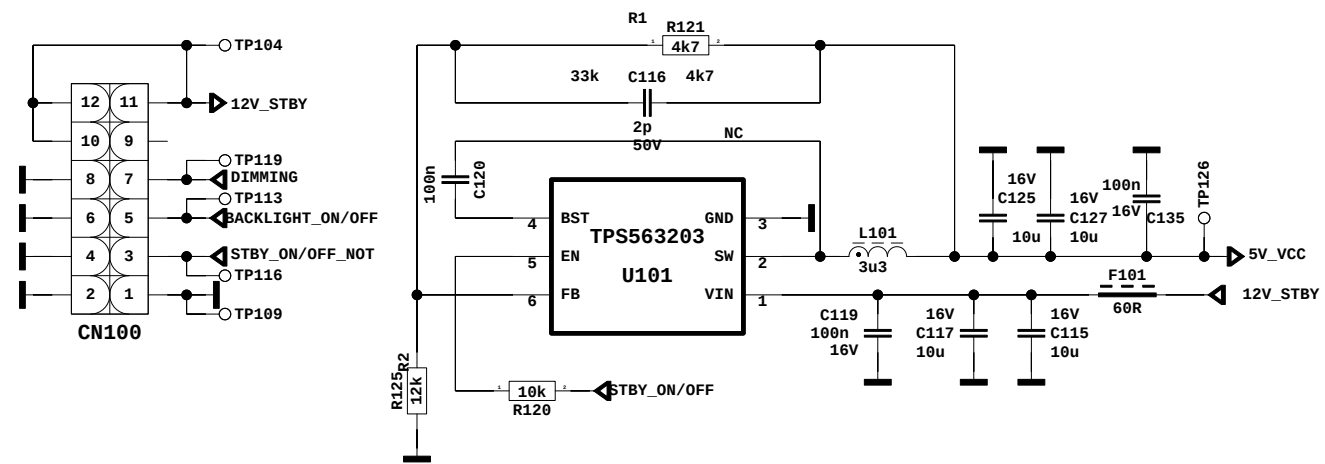


SPDIF OUT

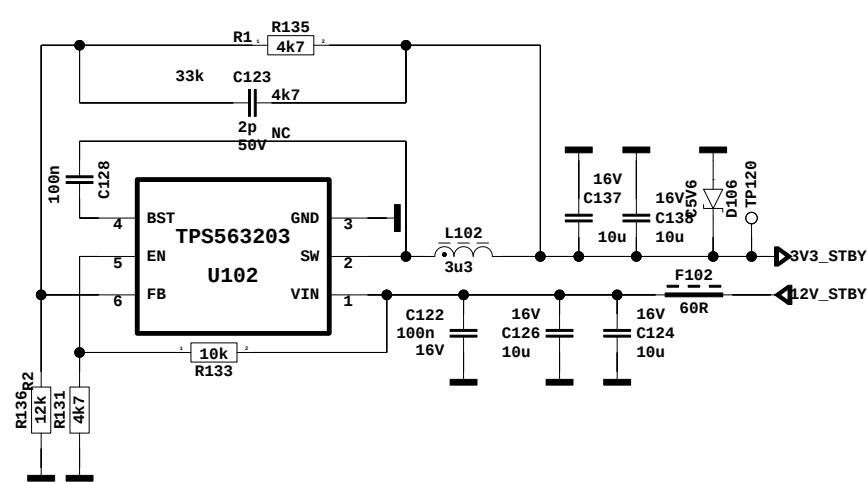




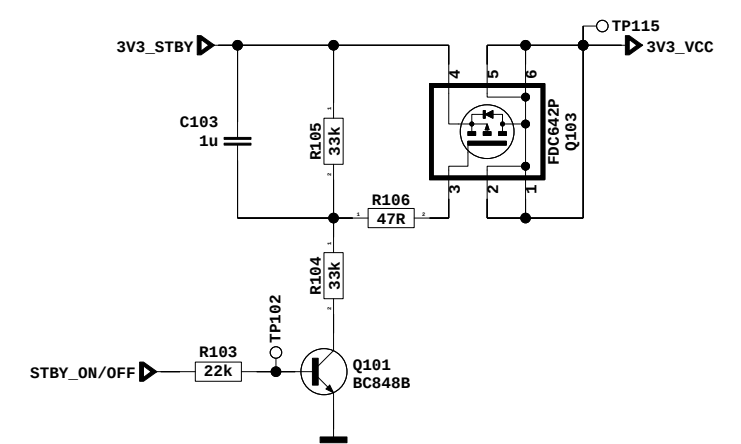
5V_VCC DC/DC (3A)



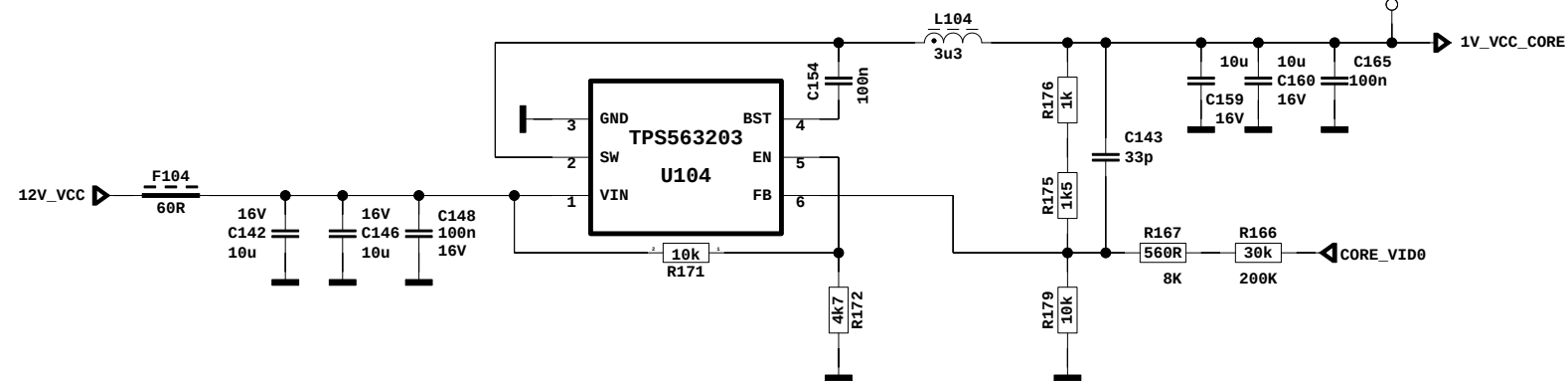
3V3_STBY DC/DC (2A)



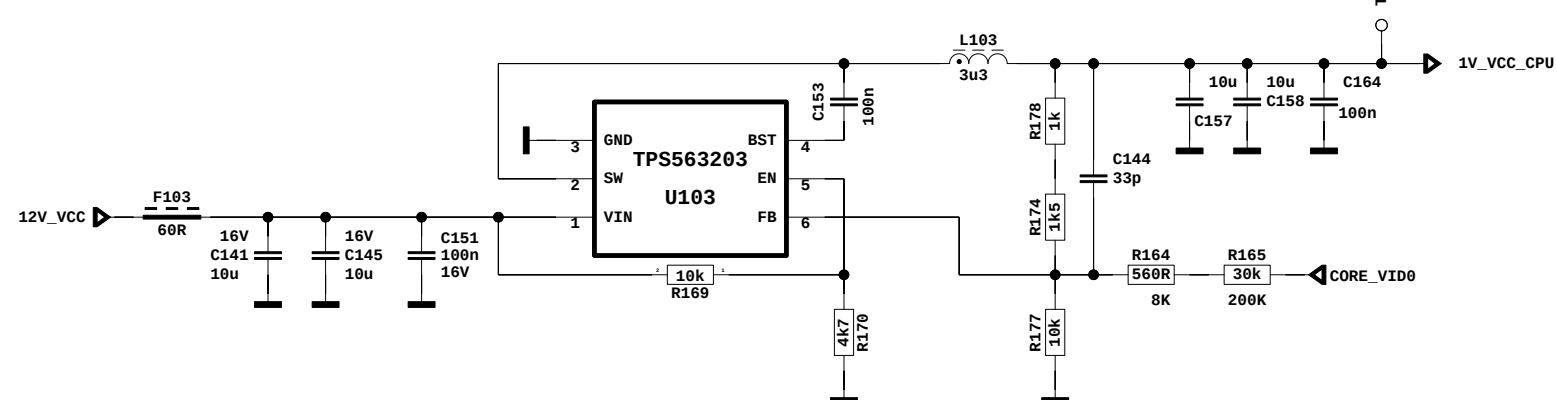
3V3_VCC SWITCH



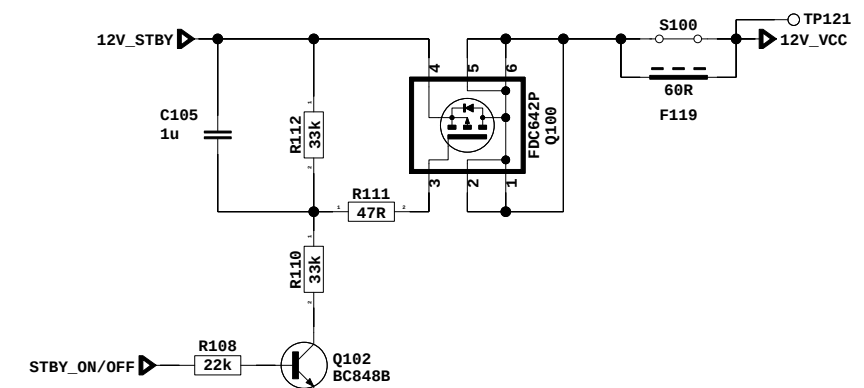
1V_VCC_CORE DC/DC (3A)



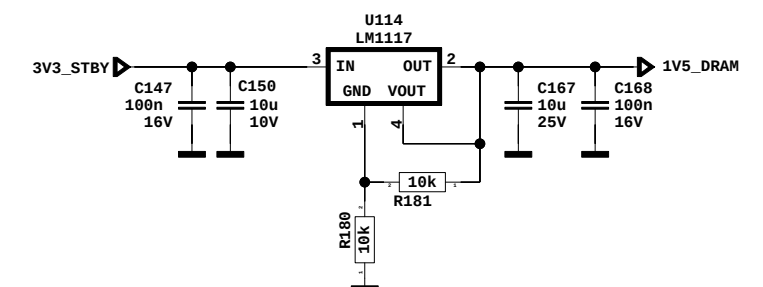
1V_VCC_CPU DC/DC (2A)



12V_VCC SWITCH



1V5_RAM LDO



1V8_VCC LDO

